

Compal Confidential

Model Name : BIZY1  
File Name : LA-D131PR10  
BOM P/N:43xxxxxxx

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BIZY1 M/B Schematic Document

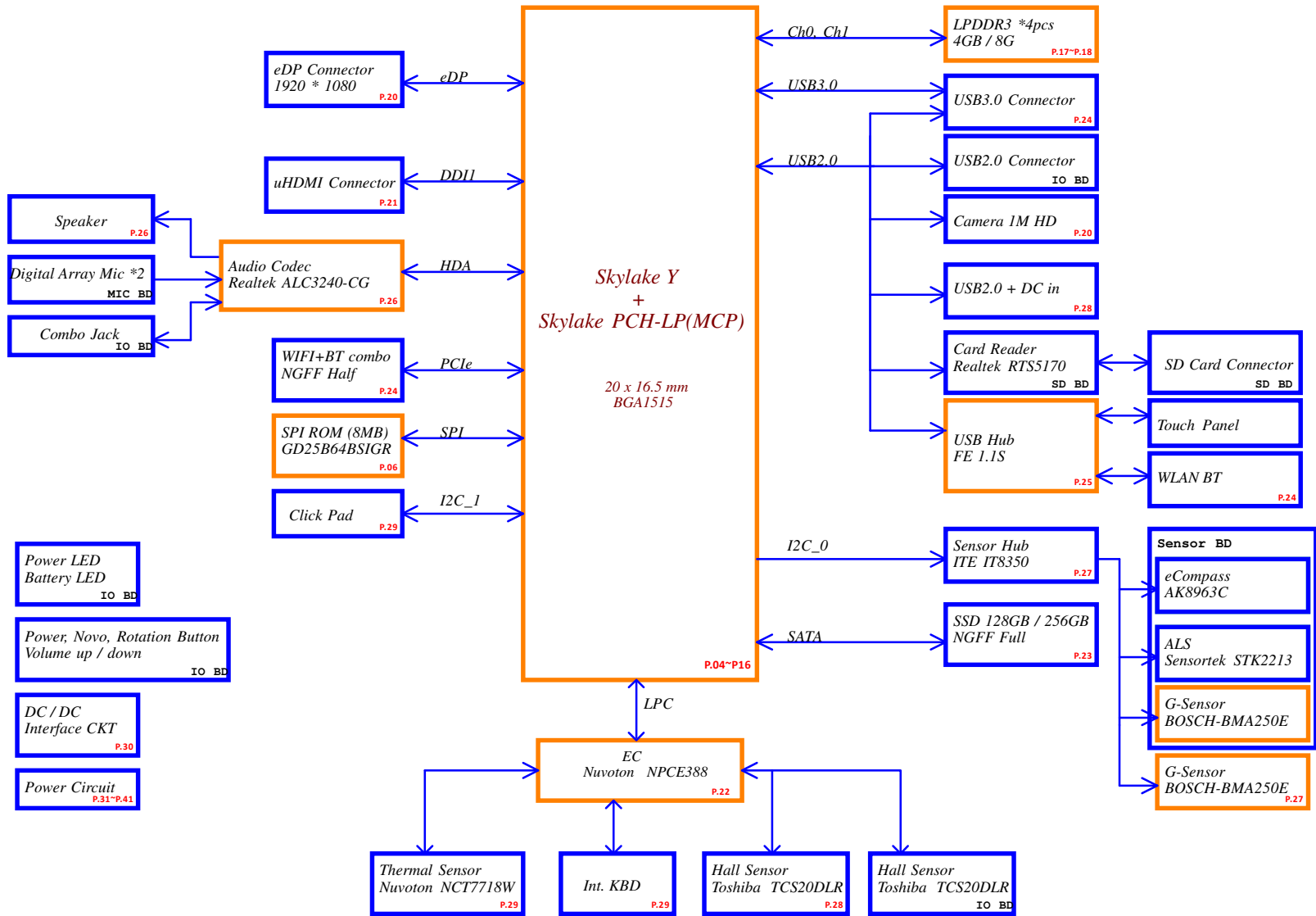
Intel skylake Y processor

2015-08-12

REV:1.0

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Paganini Intel Skylake Y Block Diagram



## Voltage Rails

power plane	State	B+	+5VALW +3VALW +1.8VALW +1.0VALW	+1.2V_VDDQ +1.8V_MEM +1.0VS_VCCST +1.0VS_VCCIO	+5VS +3VS +1.8VS +1.0VS_VCCSTG +1.0VS_VCCIO +VCC_CORE +VCC_GT +VCC_SA +0.6VS_VTT
S0		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		X	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
76 LEVEL	X76@
UNPOP	@
CPU OPTION	
DRAM Option	S4G@ H4G@ M4G@ S8G@ H8G@ M8G@
EMI POP	EMI@
ESD POP	ESD@
EMI UNPOP	@EMI@
ESD UNPOP	@ESD@
45 LEVEL	45@

## USB 2.0 Port Table

Port	USB 2.0 Port
1	USB 3.0/2.0 Port (MB)
2	USB 2.0 Port(Sub)
3	Camera
5	USB Hub
7	Card reader RTS5170
9	DCIN-USB

## USB 3.0 Port Table

Port	USB 3.0 Port
1	USB 3.0 Port (MB)
2	
3	
4	

## PCIe Port Table

Port	Lane	
1		
2		
3		
4		
5	2	
	3	
6		NGFF WLAN

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery			1001100x
Charger			
Home Key Button(TS)			

## EC SM Bus2 address

## CPU SM Bus address

Device	Address	Device	Address
NA		NA	

## CPU SML0 Bus address

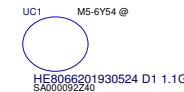
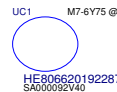
## SMBUS Control Table

	HOST	Charger	BATT	NPCE388	CPU	HomeKey	Thermal sensor NCT7718W
EC_SMB_CK1	NPCE388	+3VLP	+3VLP	X	X	+3VALW	X
EC_SMB_DA1	+3VLP	X	X	X	X	X	X
EC_SMB_CK2	NPCE388	+3VS	X	X	X	+3VS	X
EC_SMB_DA2	+3VS	X	X	X	X	X	X
SMBCLK	CPU	+3VALW	X	X	X	X	X
SMBDATA	+3VALW	X	X	X	X	X	X
SML0CLK	CPU	+3VALW	X	X	X	X	X
SML0DATA	+3VALW	X	X	X	X	X	X
SML1CLK	CPU	+3VS	X	X	X	X	X
SML1DATA	+3VS	X	X	X	X	X	X

## HDMI Logo



## CPU part



## PCB part



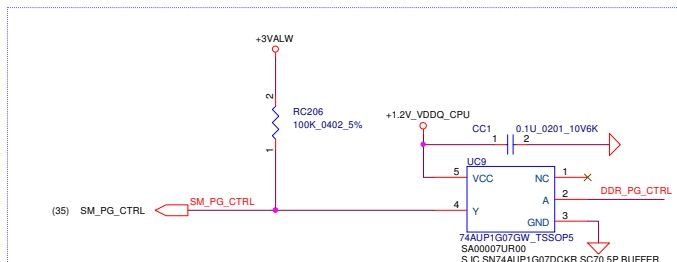
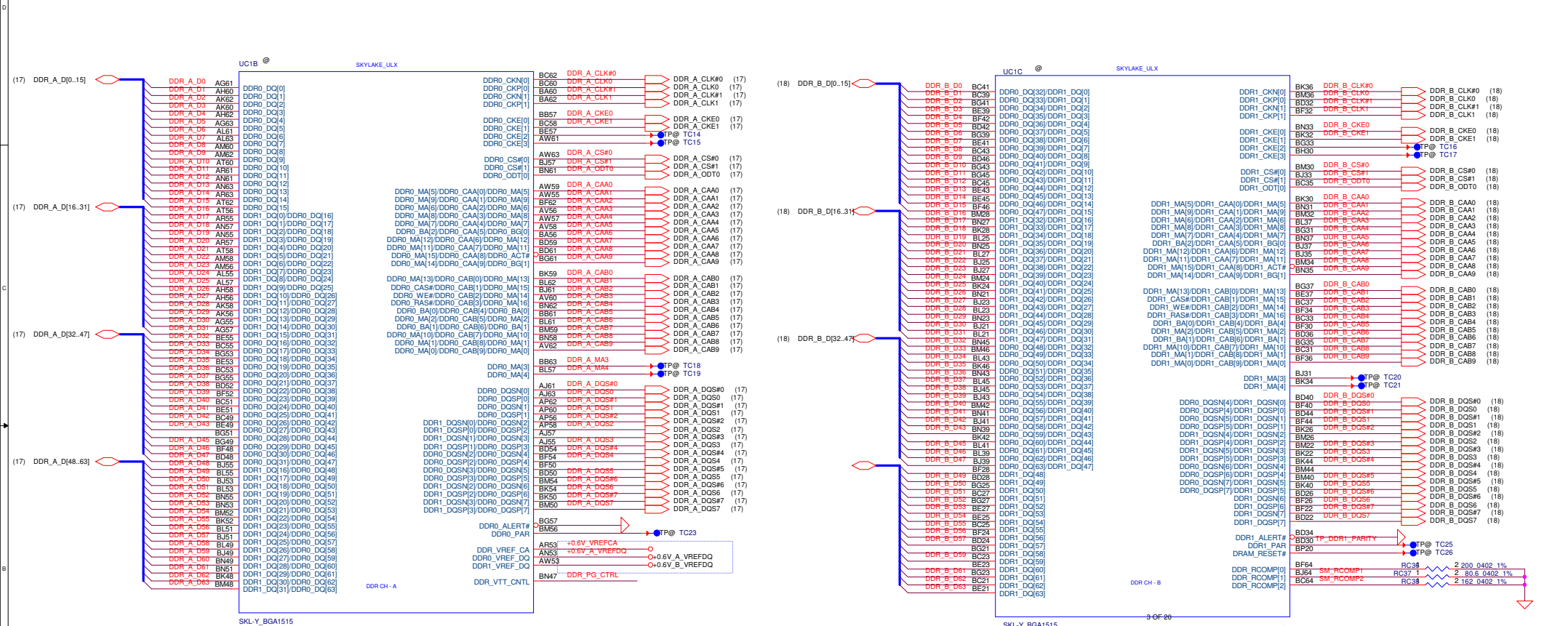
## DRAM



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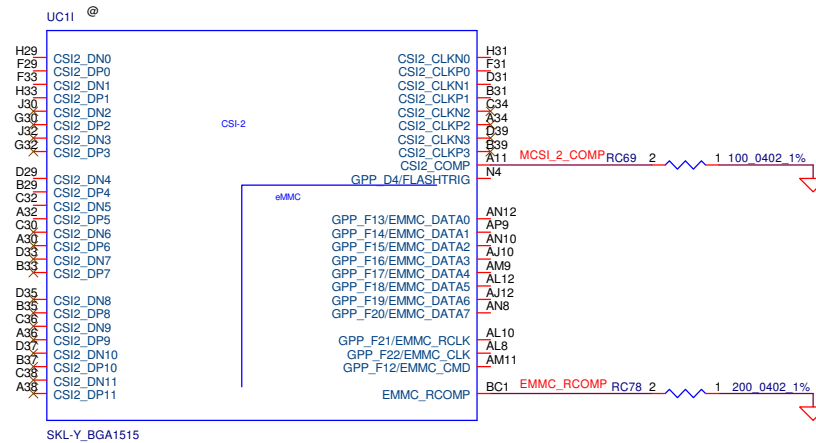
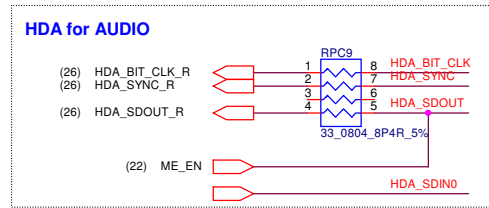
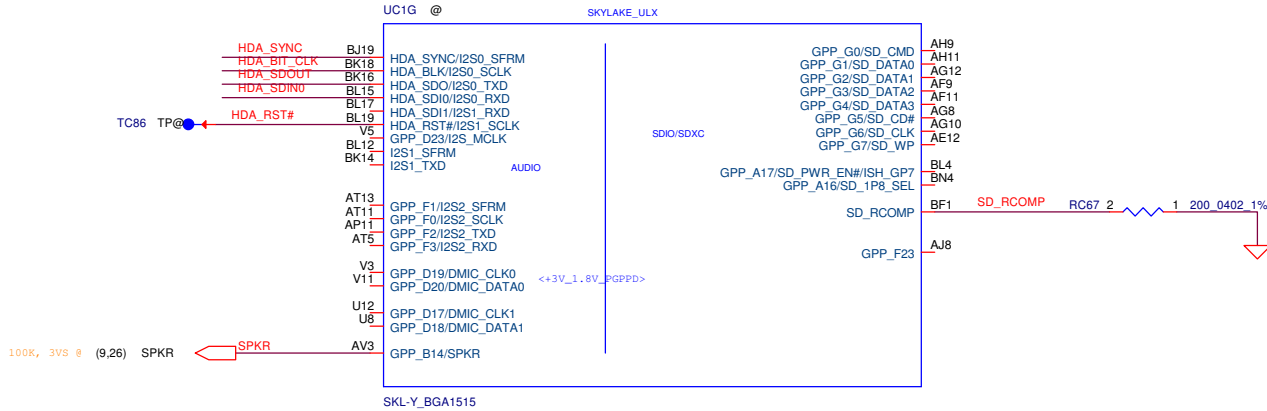


# Interleaved Memory



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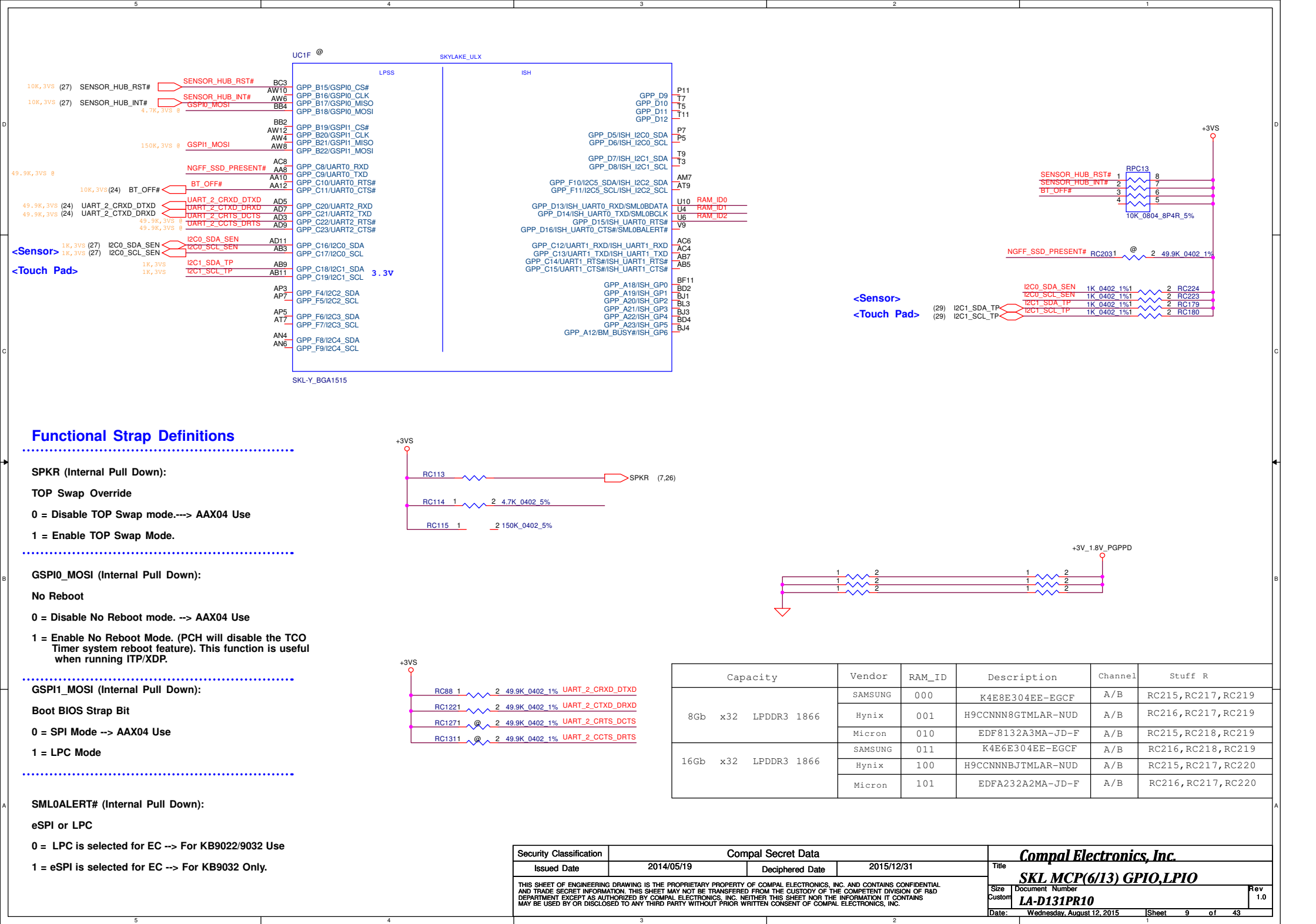
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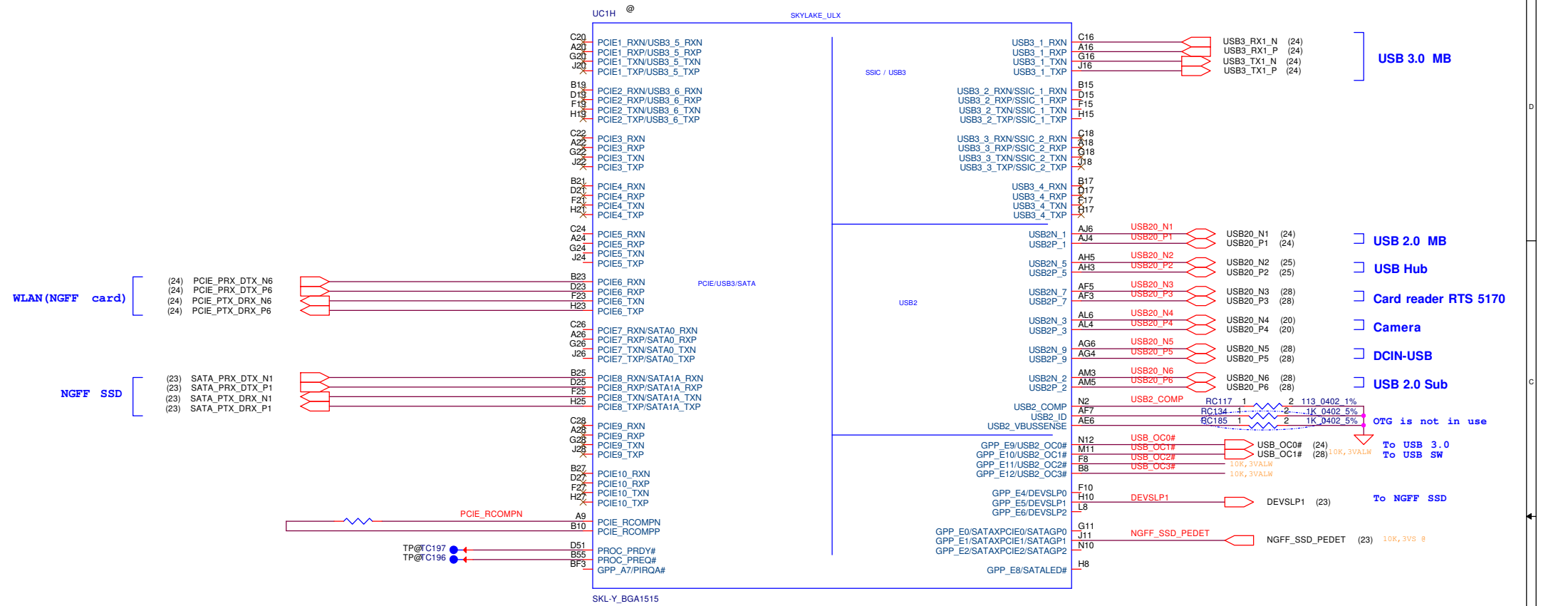
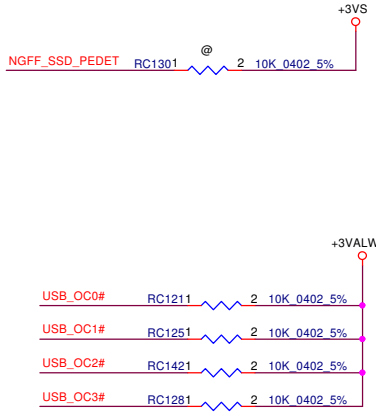
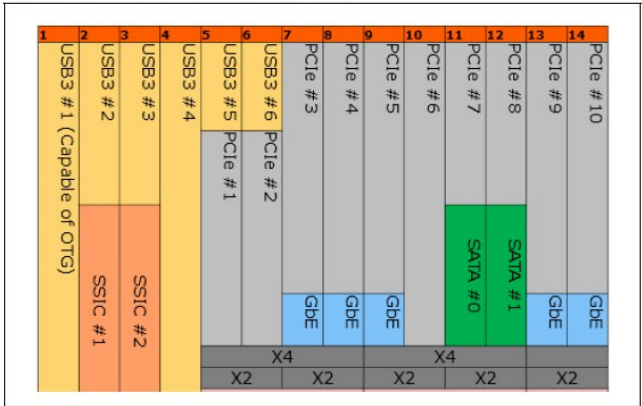
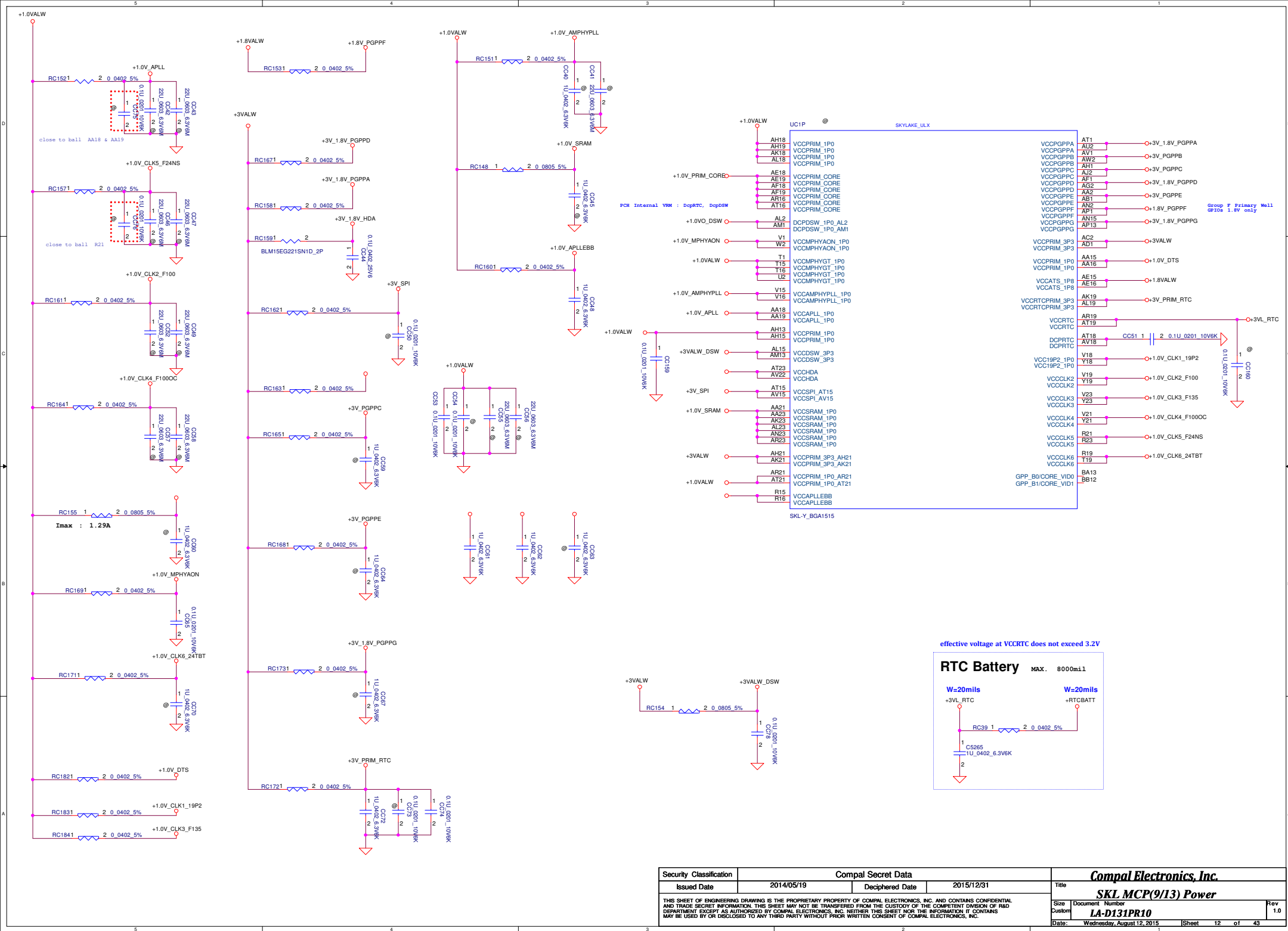


Figure 11-2. High Speed I/O (HSIO) Lane Multiplexing in SKL Y

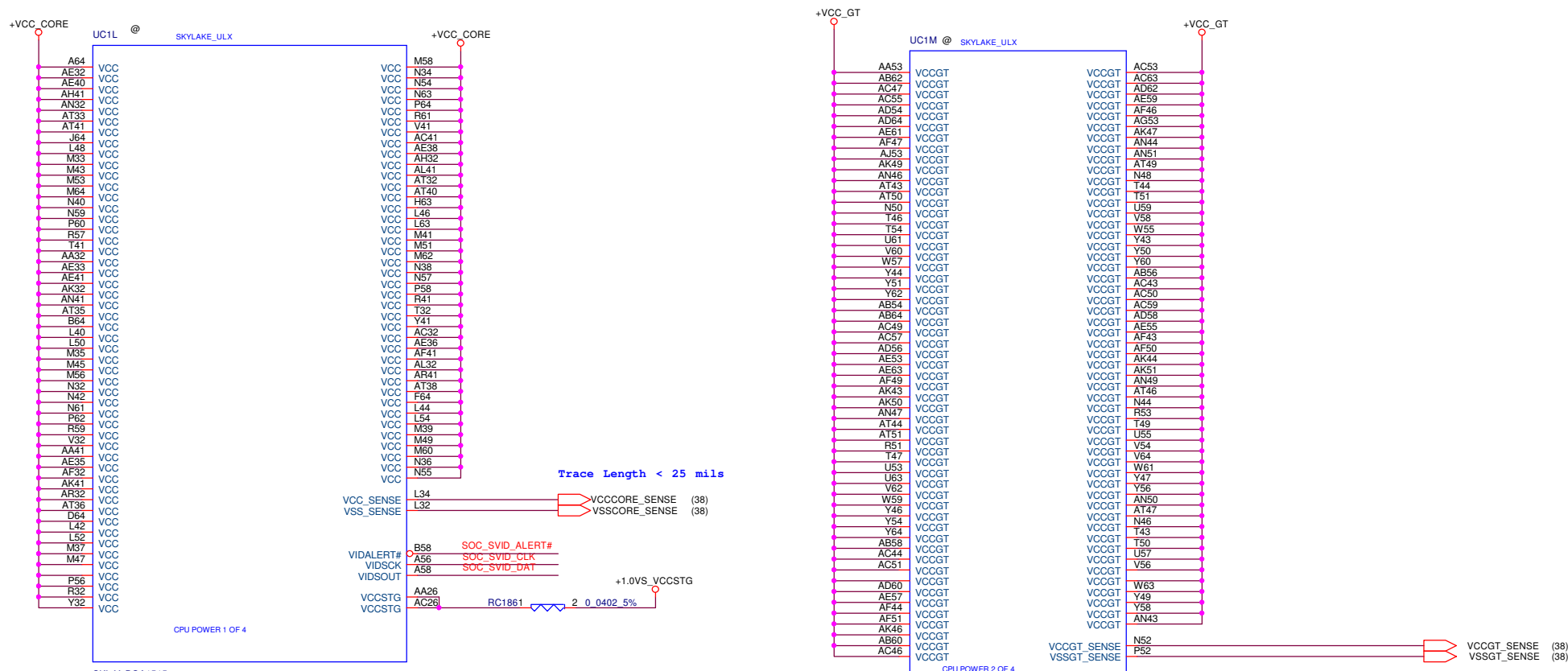


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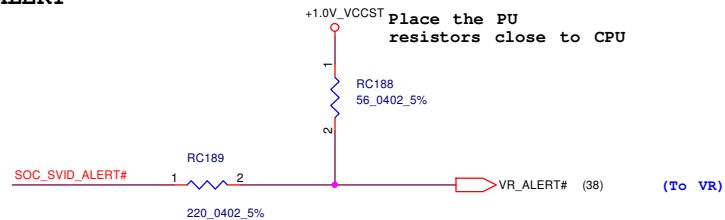




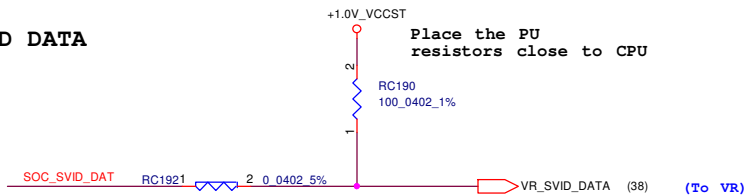
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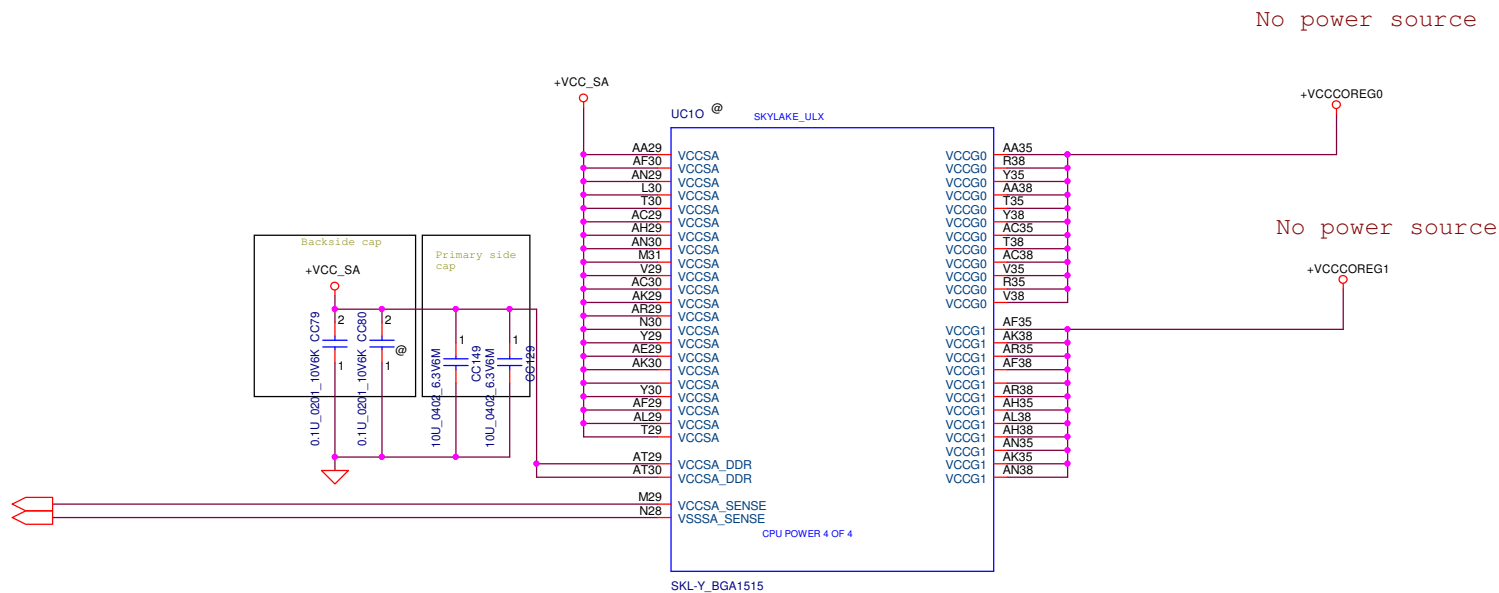
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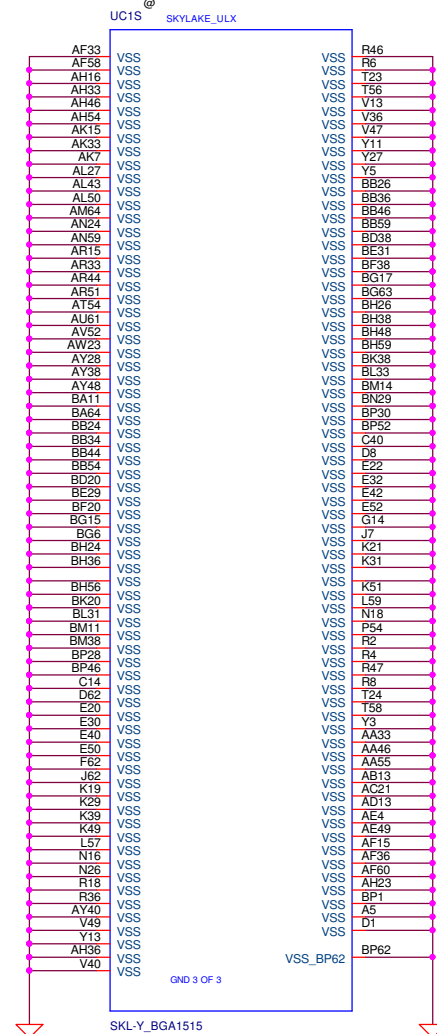
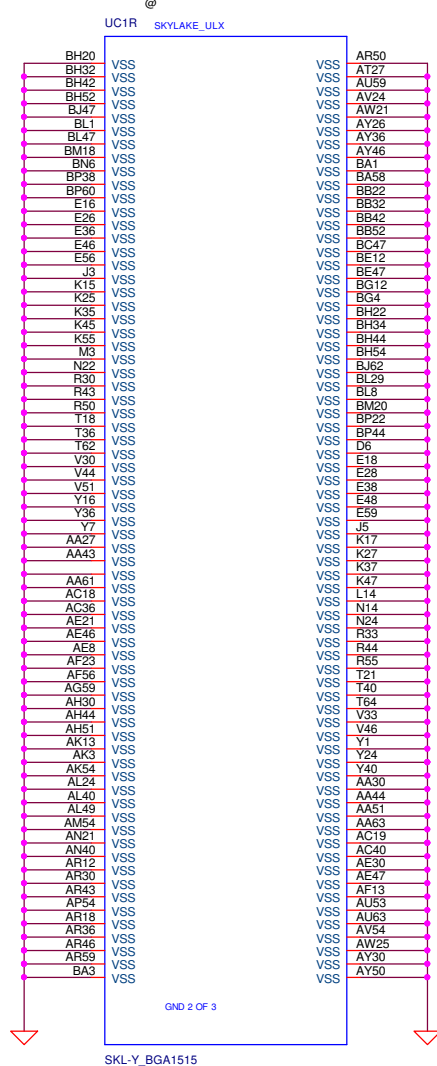
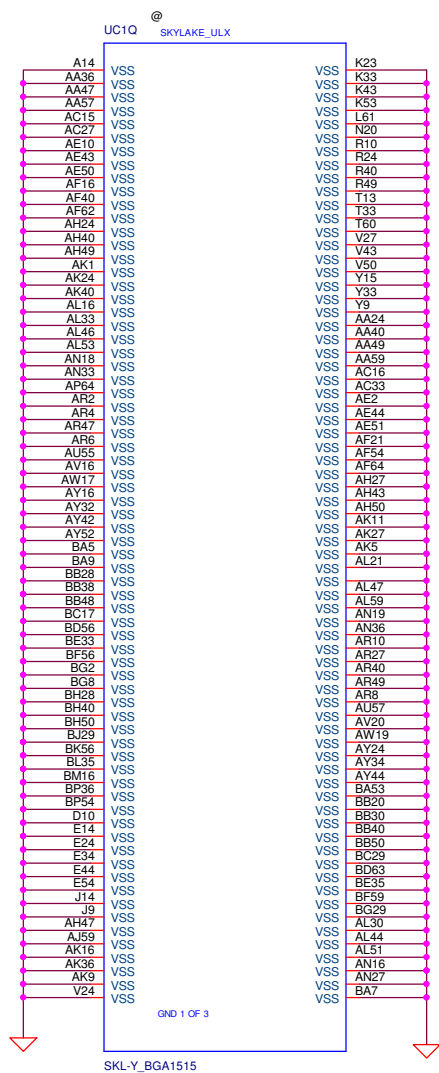
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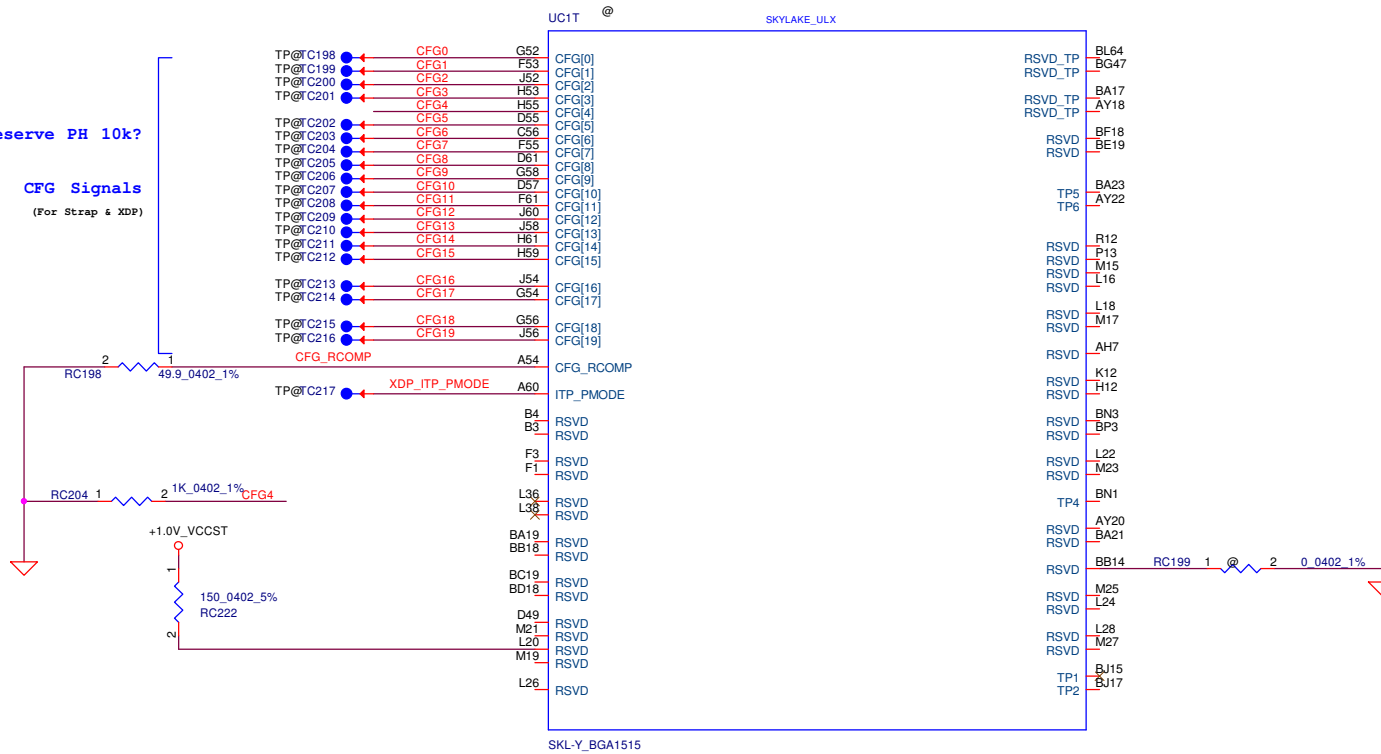
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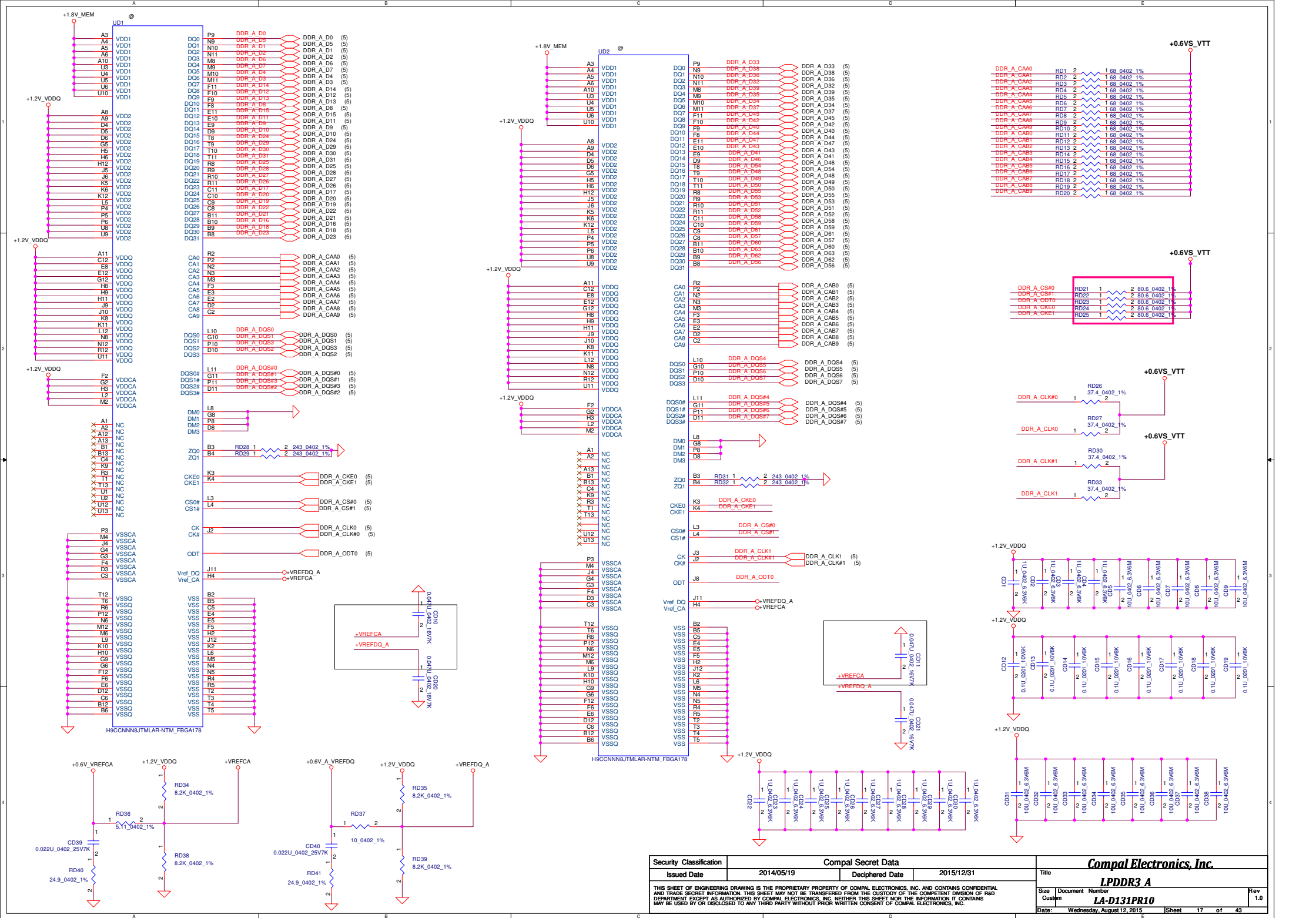
CRB : Reserve PH 10k?

CFG Signals  
(For Strap & XDP)

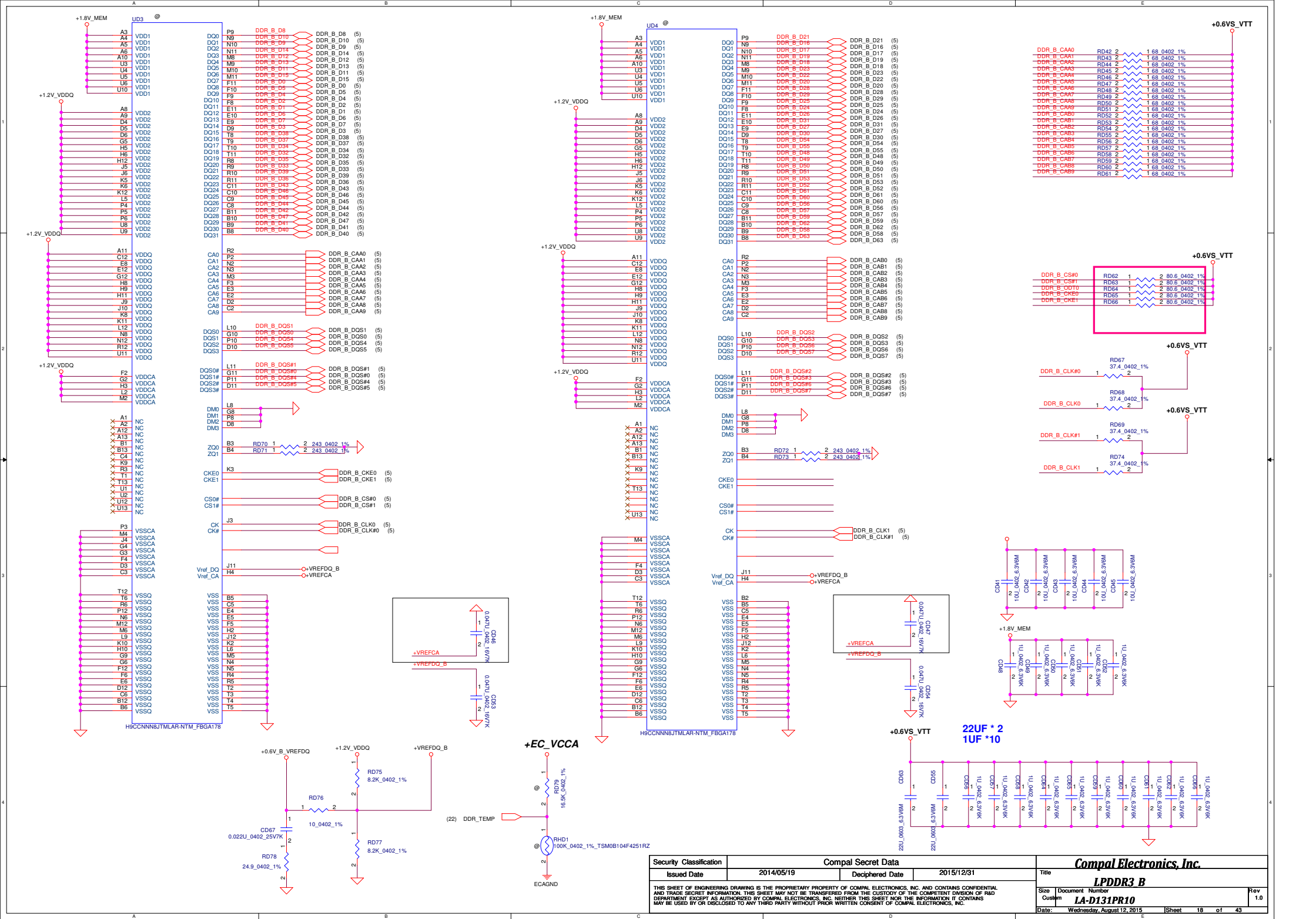


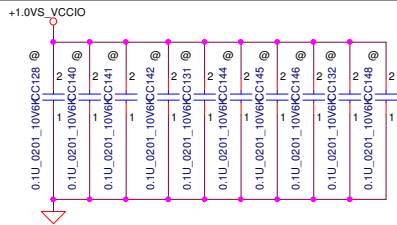
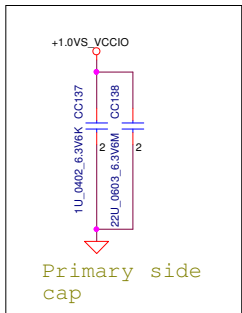
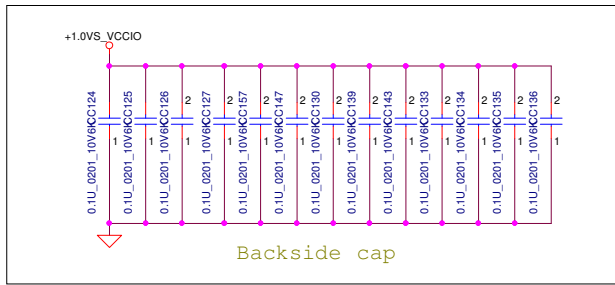
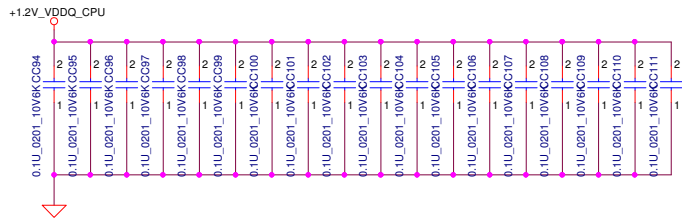
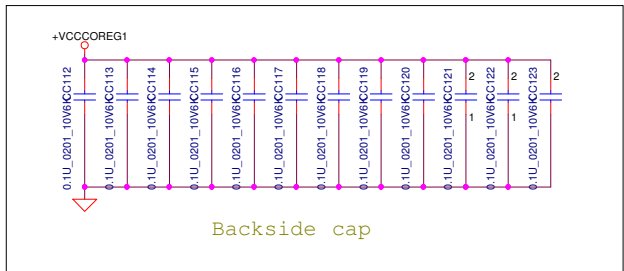
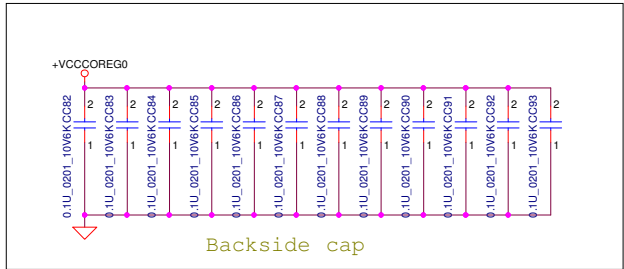
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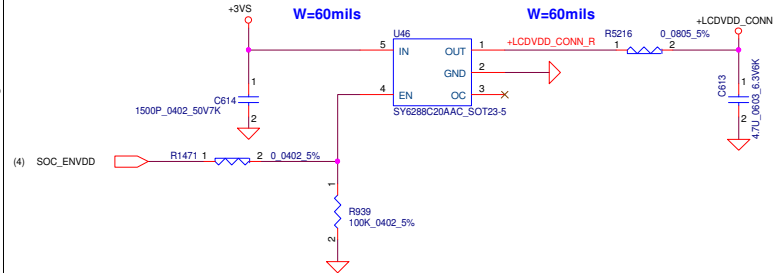
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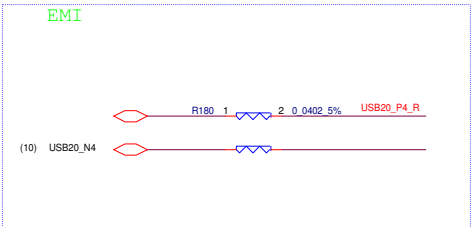
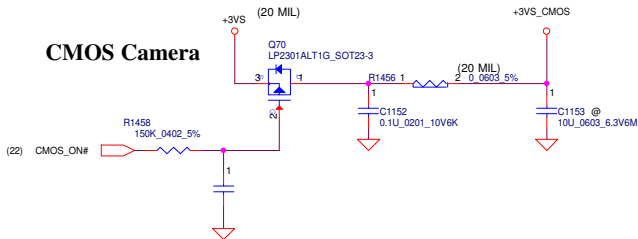


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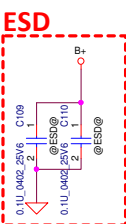
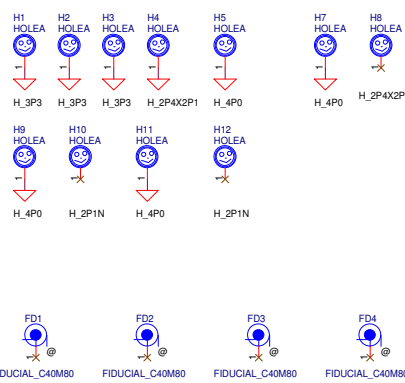
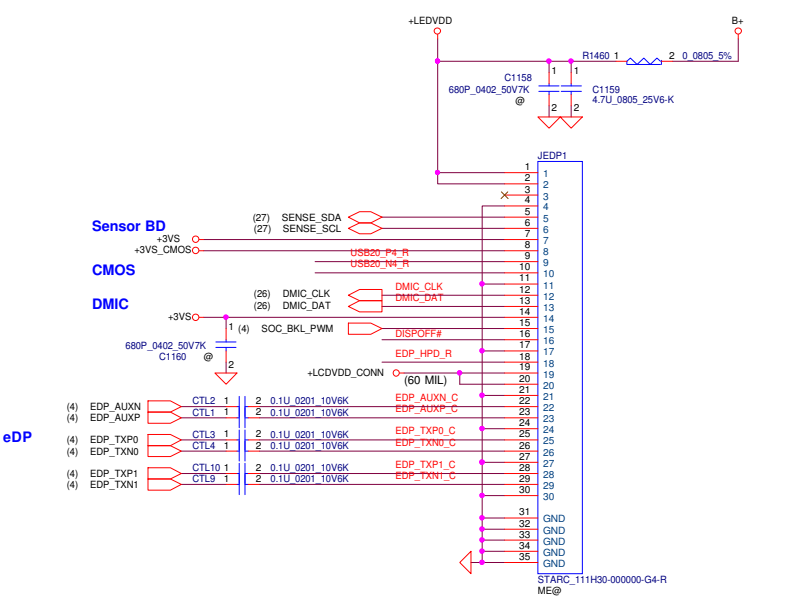
LCD POWER CIRCUIT



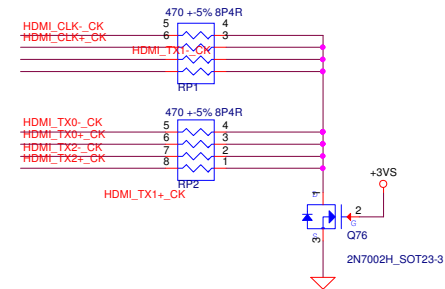
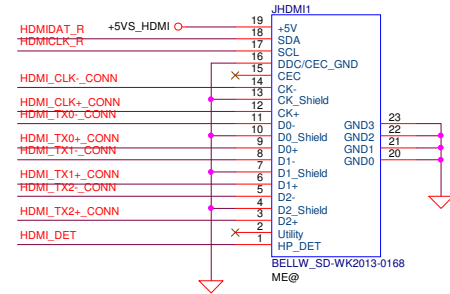
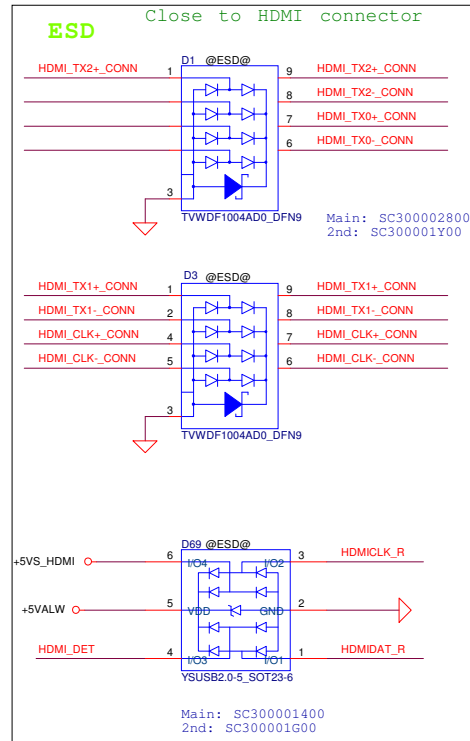
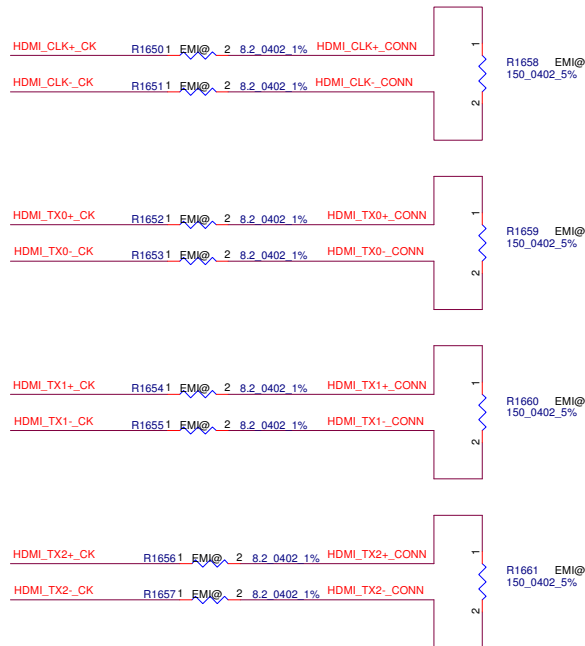
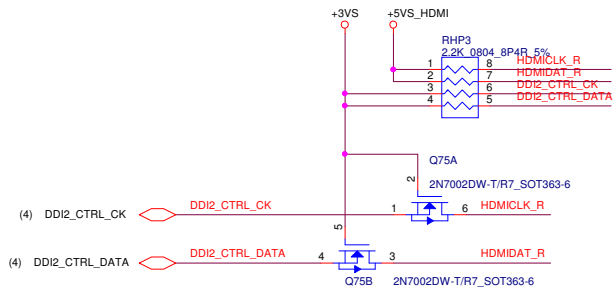
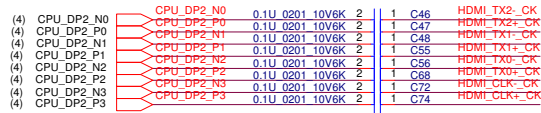
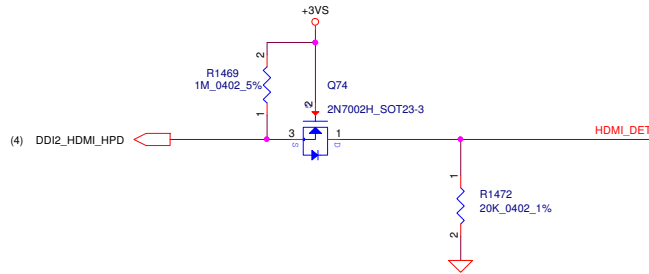
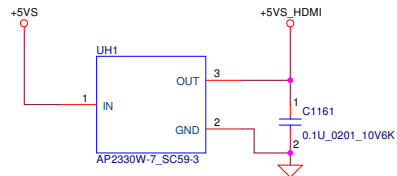
CMOS Camera



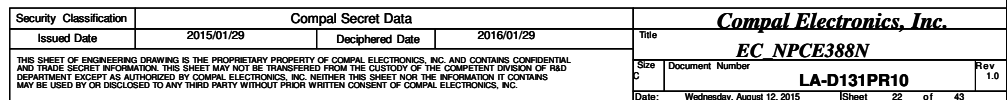
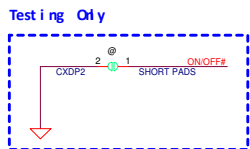
eDP PANEL/DMIC/COMS/SENSOR. Conn.



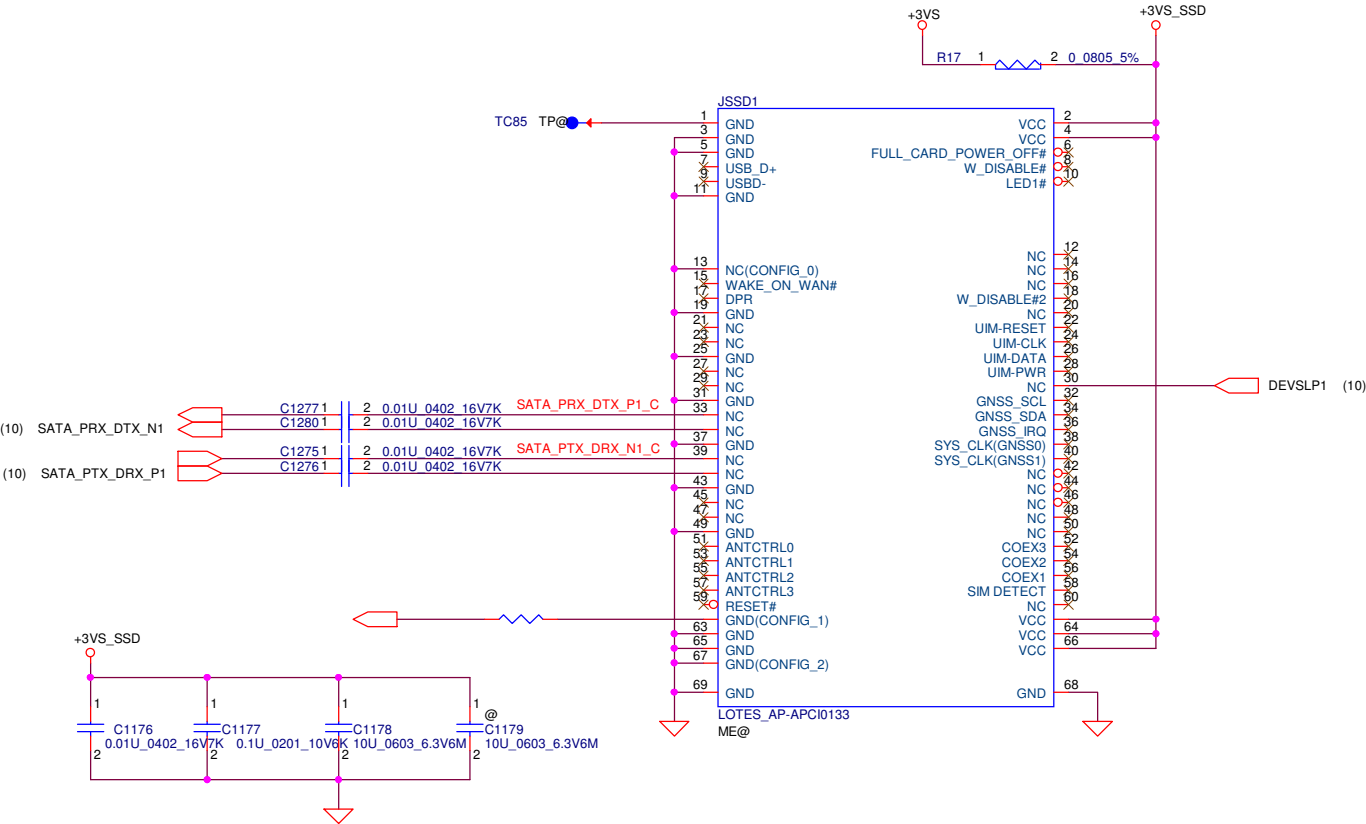
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Deciphered Date				2017/04/10				HDMI CONN			
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				Document Number				1 Sheet			
				LA-D131PR10				21 of 43			
				Rev 1.0							

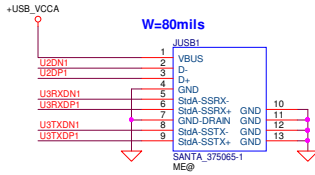
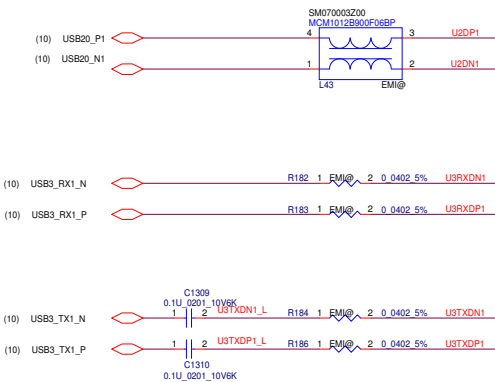
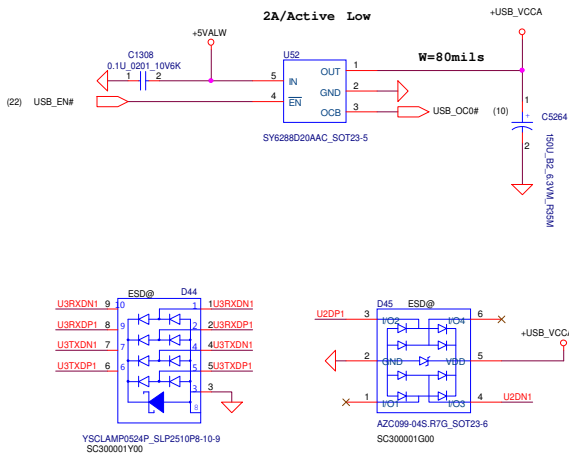


NGFF for SSD(Key B)



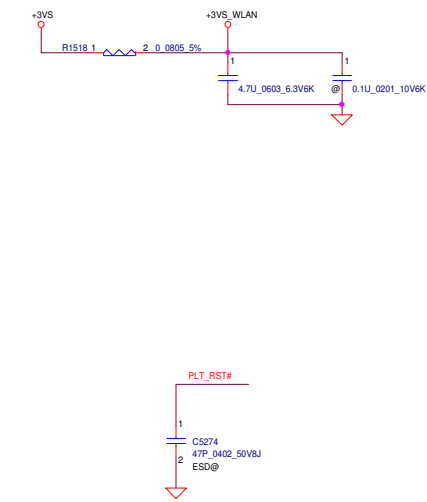
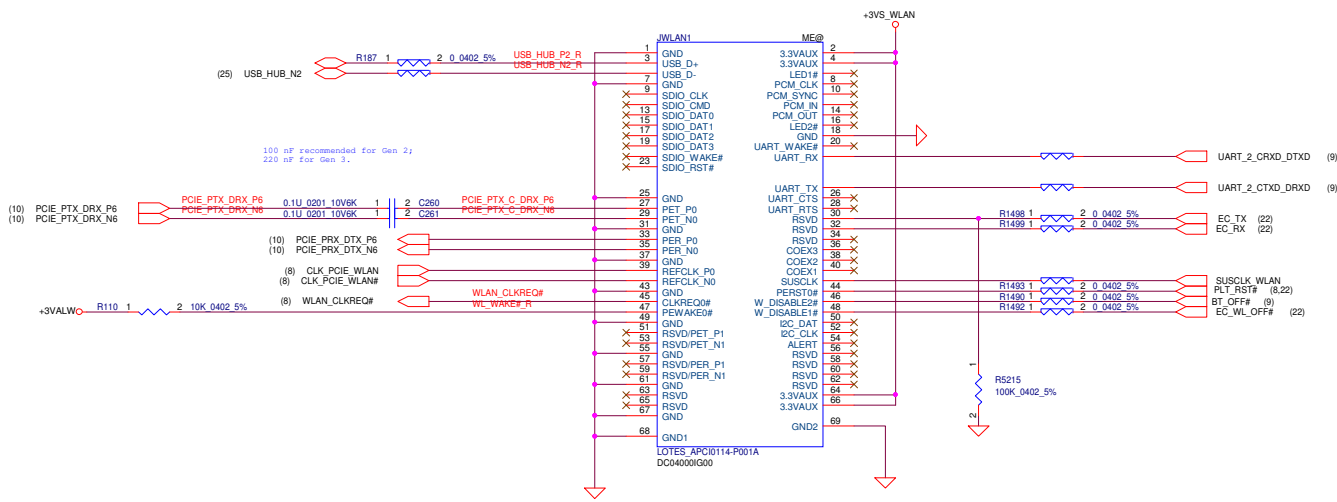
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Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	
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USB 3.0 Conn.



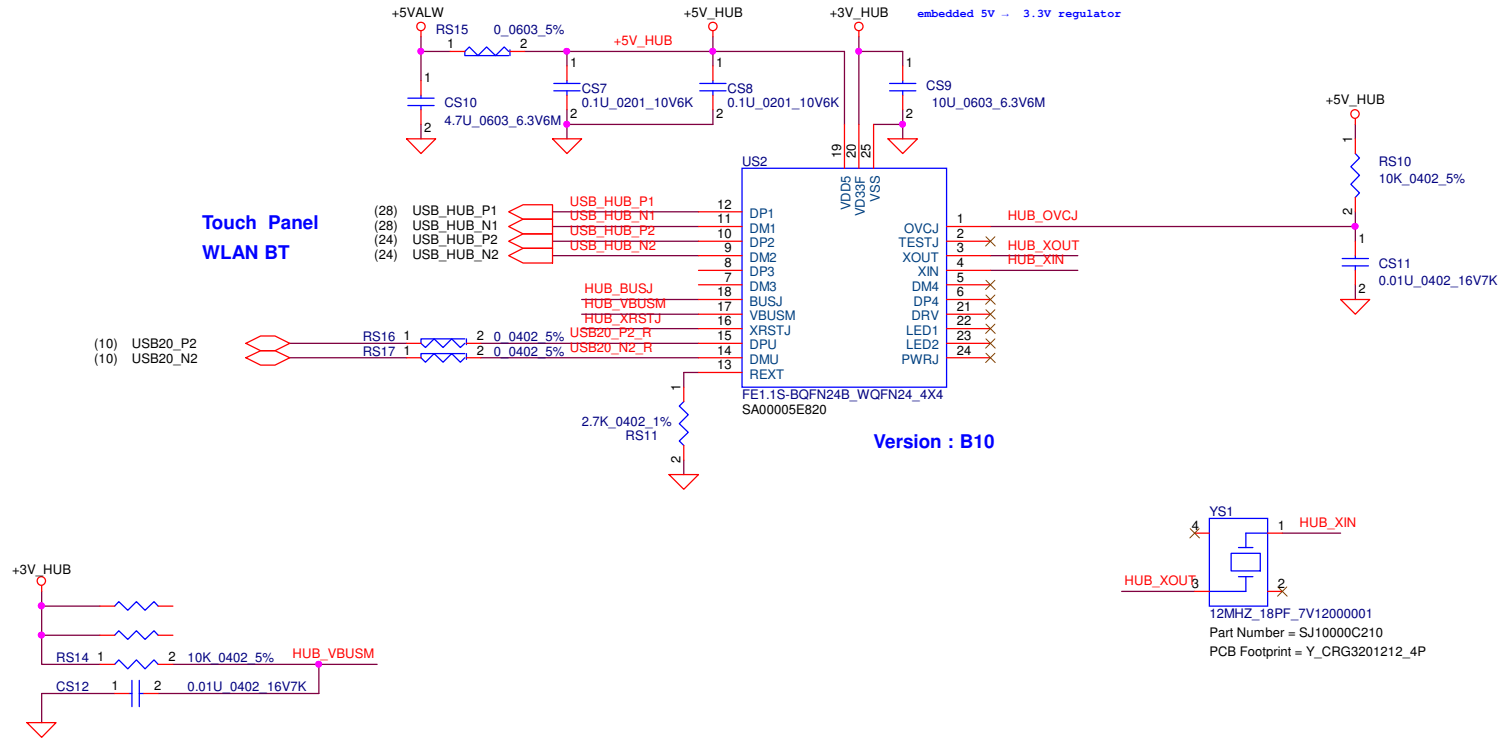
Place TX AC coupling Cap (C843-C850). Close to connector

NGFF for WLAN(Key E)



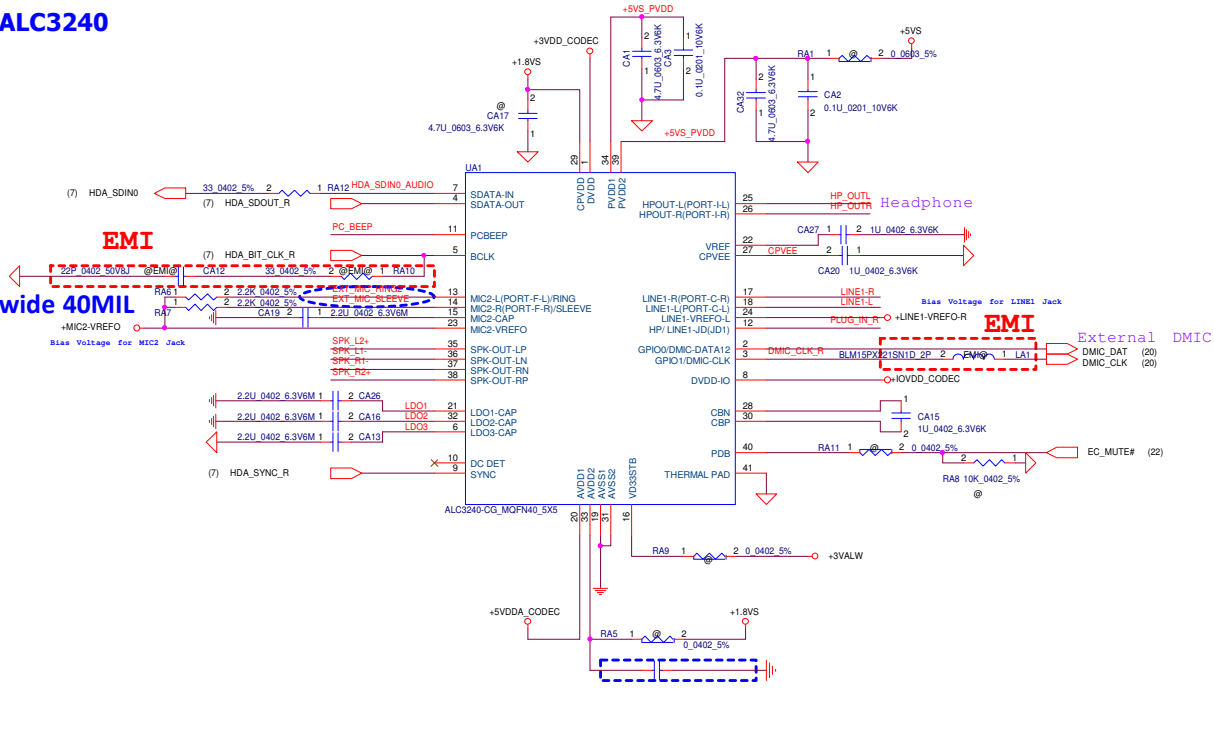


# USB2.0 HUB

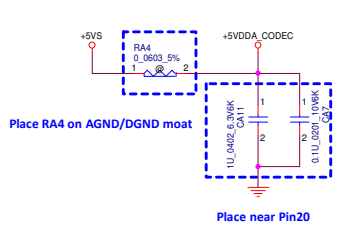


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Size	Document Number	LA-D131PR10		Rev	1.0
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ALC3240



+5VS → +5VDDA\_CODEC



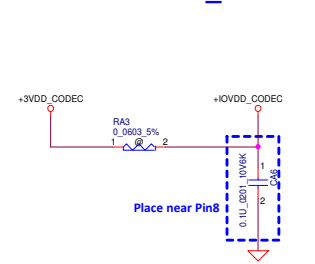
Each Platf or m Power Net Support list:

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
AMD Carrizo	V	V	V	V	V
AMD Carrizo-L	V	V	V	V	V
Intel Broadwell	V	V	V	V	V
Intel Braswell	V	V	V	V	V
Intel Skylake	V	V	V	V	V
Intel Bay trail-M	V	V	V	V	V

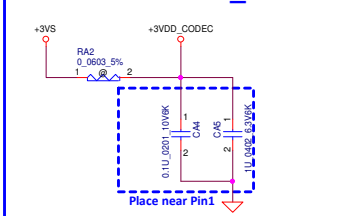
Each Platf or m HDA link Voltage Support (R n 8):

	3.3V	1.5V
AMD Carrizo		V
AMD Carrizo-L		V
Intel Broadwell	V	V
Intel Braswell		V
Intel Skylake	V	V
Intel Bay trail-M		V

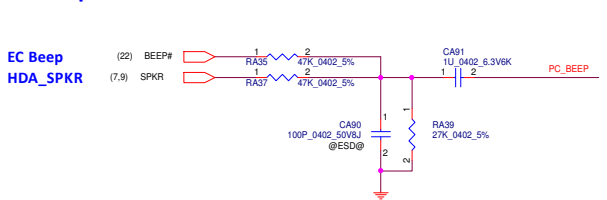
+3VDD\_CODEC → +IOVDD\_CODEC



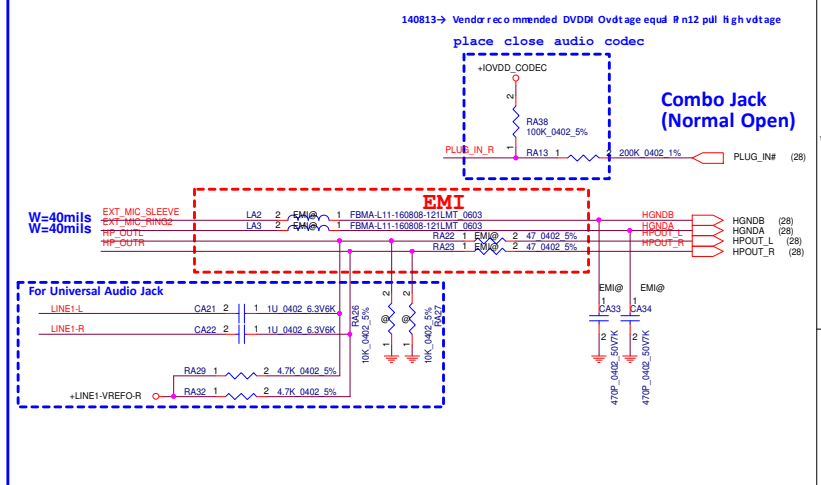
+3VS → +3VDD\_CODEC



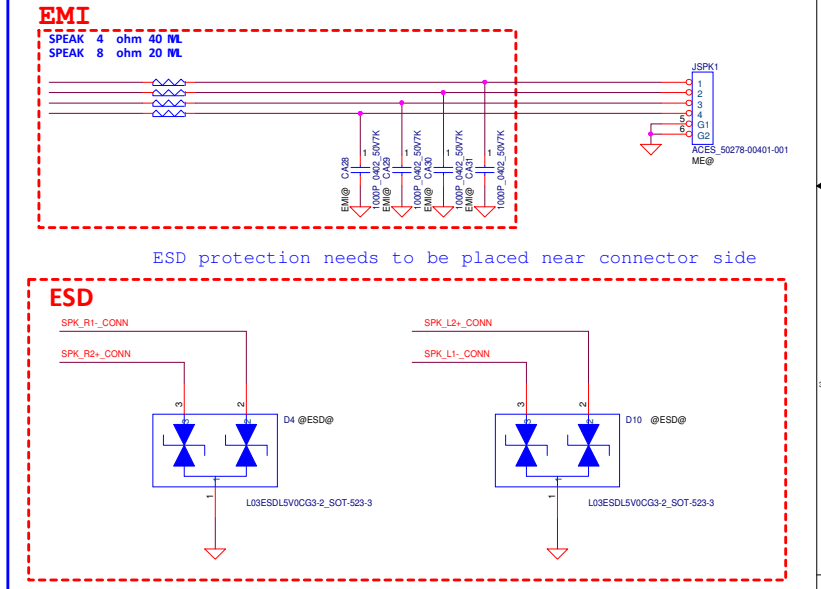
PC BEEP



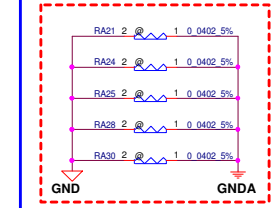
Input



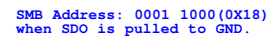
Output



EMI

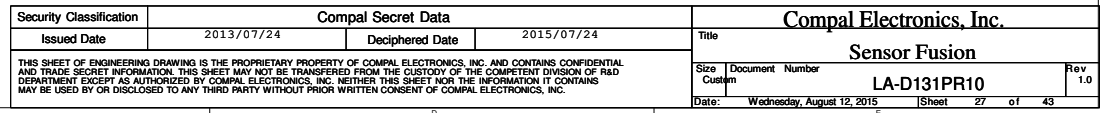


2nd G-sensor

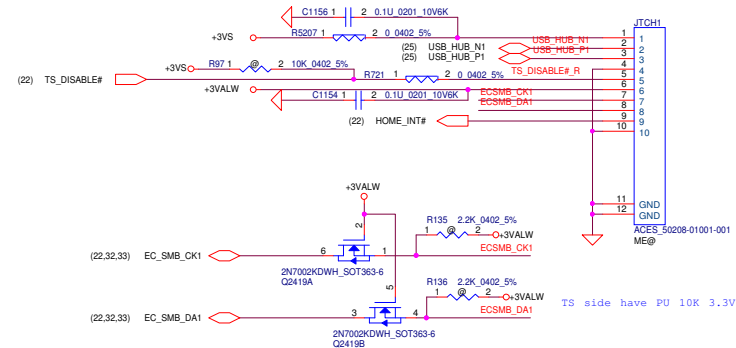
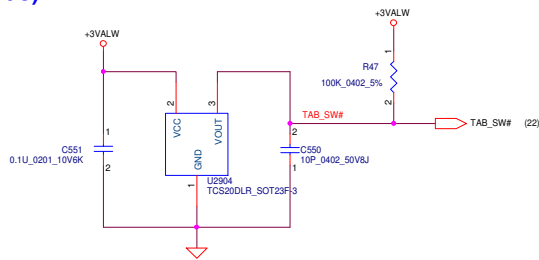


Schematic diagram of the BMA250E\_LGA12 pin connections. The chip is shown with its 12 pins. Pin 1 is connected to +3VS. Pin 2 is connected to GND. Pin 3 is connected to +3VS. Pin 4 is connected to GND. Pin 5 is connected to GND. Pin 6 is connected to GND. Pin 7 is connected to GND. Pin 8 is connected to GND. Pin 9 is connected to GND. Pin 10 is connected to GND. Pin 11 is connected to GND. Pin 12 is connected to GND. The chip is labeled UGS3 @, CGS5 0.1U\_0201\_10V6K, CGS6 0.1U\_0201\_10V6K, and BMA250E\_LGA12. The pin connections are: 1: +3VS, 2: GND, 3: +3VS, 4: GND, 5: GND, 6: GND, 7: GND, 8: GND, 9: GND, 10: GND, 11: GND, 12: GND.

## Sensor Hub

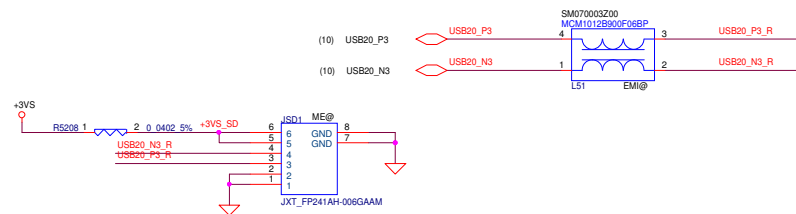


## Touch Panel



## SD Board

EMI

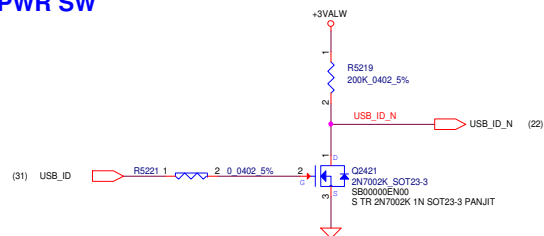


**oard**

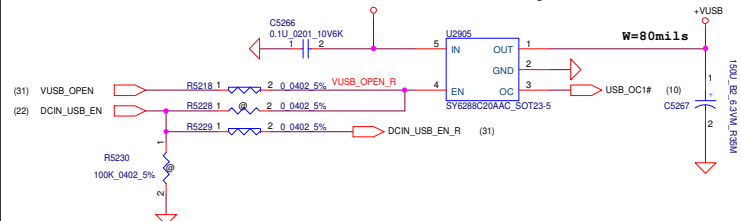
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**DCIN-USB PWR SW**

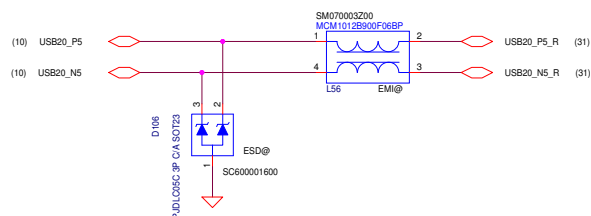


For DCIN-USB Combo port only  
2A/Active High



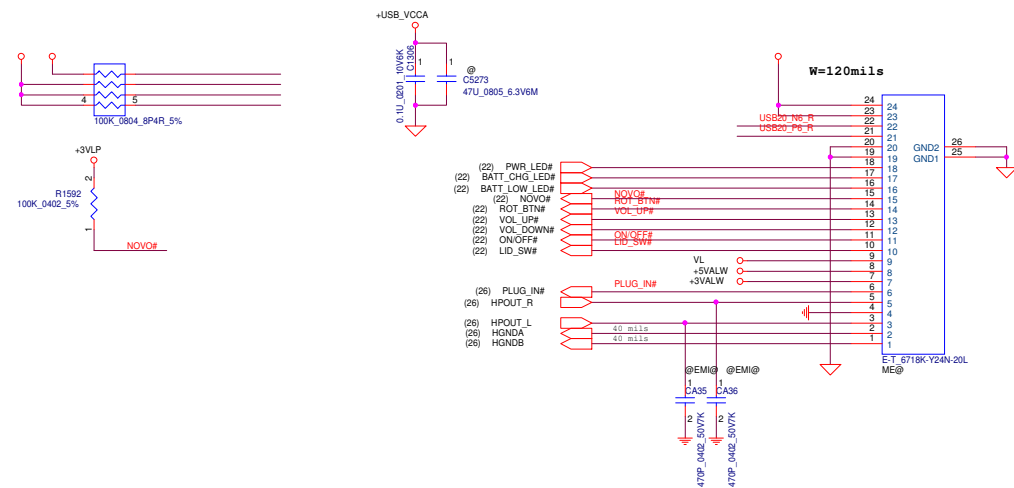
	AC S0	AC S3	AC S5
USB_ID_N	L	L	L
DCIN_USB_EN	L	L	L
VUSB_OPEN	L	L	L
	DC S0	DC S3	DC S5
USB_ID_N	H	H	L
DCIN_USB_EN	H	H	L
VUSB_OPEN	H	H	L
	DC to AC S0	DC to AC S3	DC to AC S5
USB_ID_N	H->L	H->L	L->L
DCIN_USB_EN	H->L	L->L	L->L
VUSB_OPEN	H->L	H->L	L->L
	AC to DC S0	AC to DC S3	AC to DC S5
USB_ID_N	L->H	L->H	L->L
DCIN_USB_EN	L->H	L->L	L->L
VUSB_OPEN	L->H	L->L	L->L

```
AC to DC S0
When EC get USB_ID_N L--> H, then
DCIN_USB_EN need delay 2's then L-->H
```



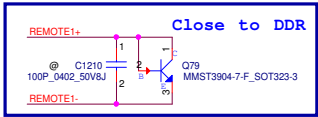
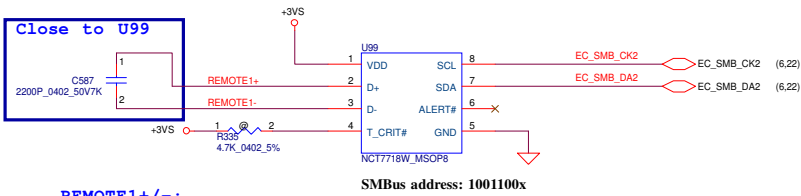
## I/O Board

EMI

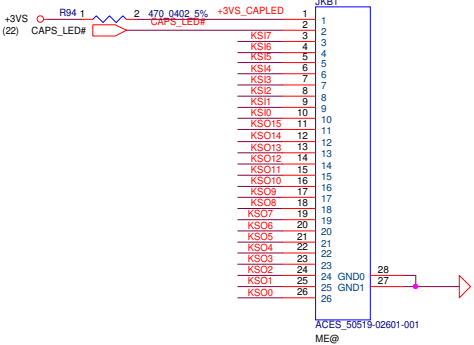
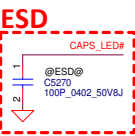
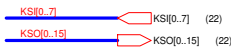


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Thermal Sensor

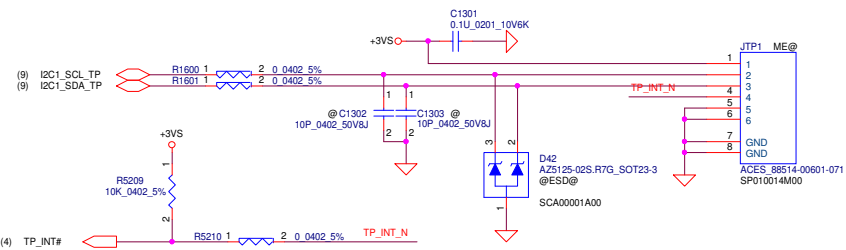


Keyboard



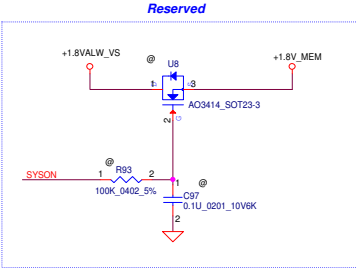
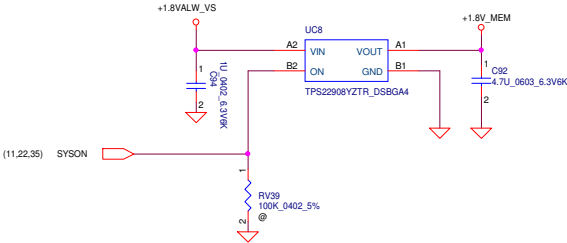
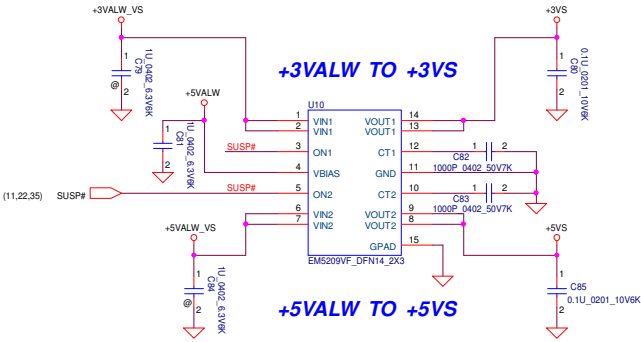
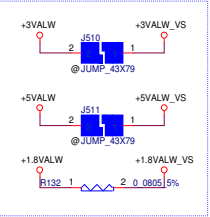
PIN1	+3VALW
PIN2	CAP_LED
PIN3	KS17
PIN4	KS16
PIN5	KS15
PIN6	KS14
PIN7	KS13
PIN8	KS12
PIN9	KS11
PIN10	KS10
PIN11	KS015
PIN12	KS014
PIN13	KS013
PIN14	KS012
PIN15	KS011
PIN16	KS010
PIN17	KS09
PIN18	KS08
PIN19	KS07
PIN20	KS06
PIN21	KS05
PIN22	KS04
PIN23	KS03
PIN24	KS02
PIN25	KS01
PIN26	KS00

Click Pad

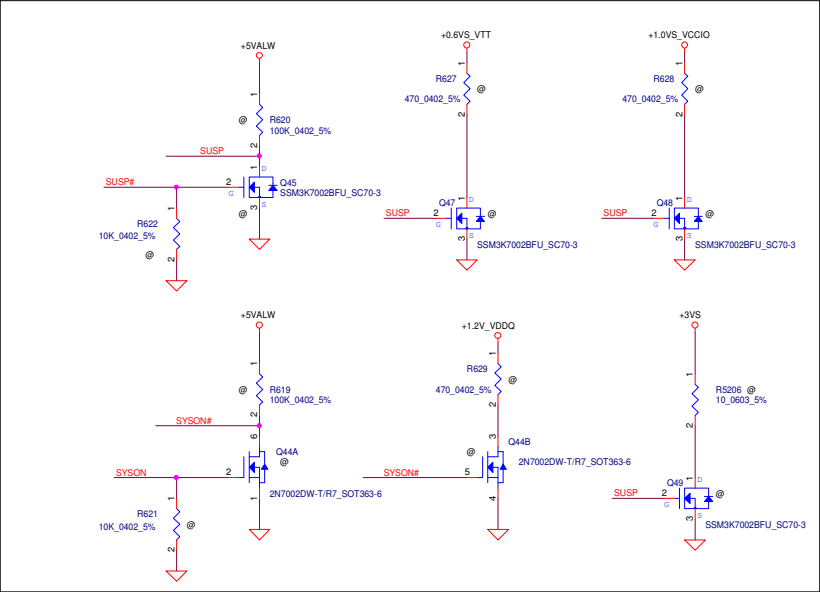


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For Power consumption Measurement

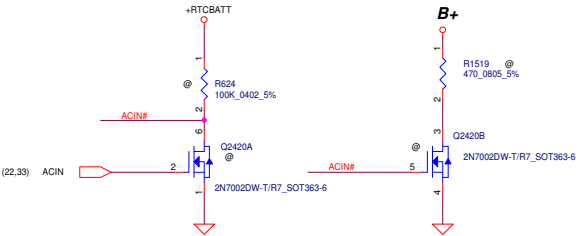


+1.8VALW TO +1.8V\_MEM

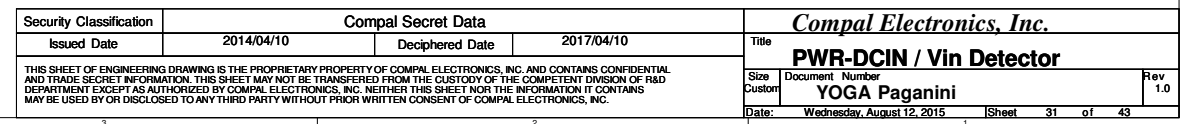


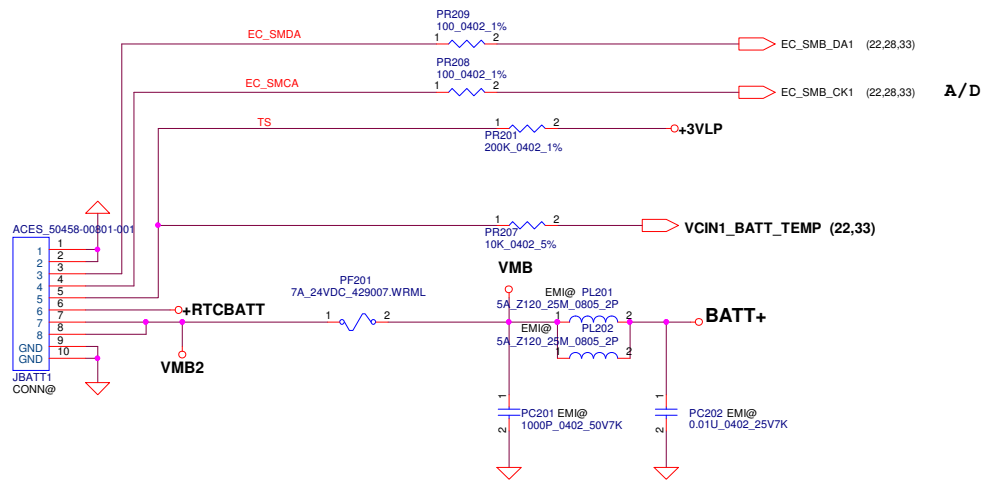
Use for panel sequence

B+ dischager



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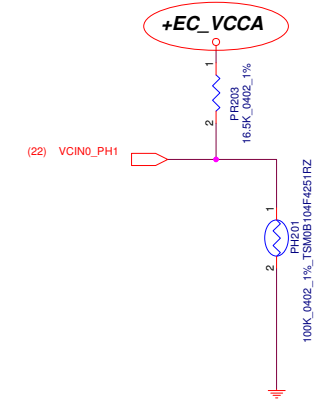




**PH201 under CPU botten side :**  
**CPU thermal protection at 93 +-3 degree C**  
**Recovery at 56 +-3 degree C**

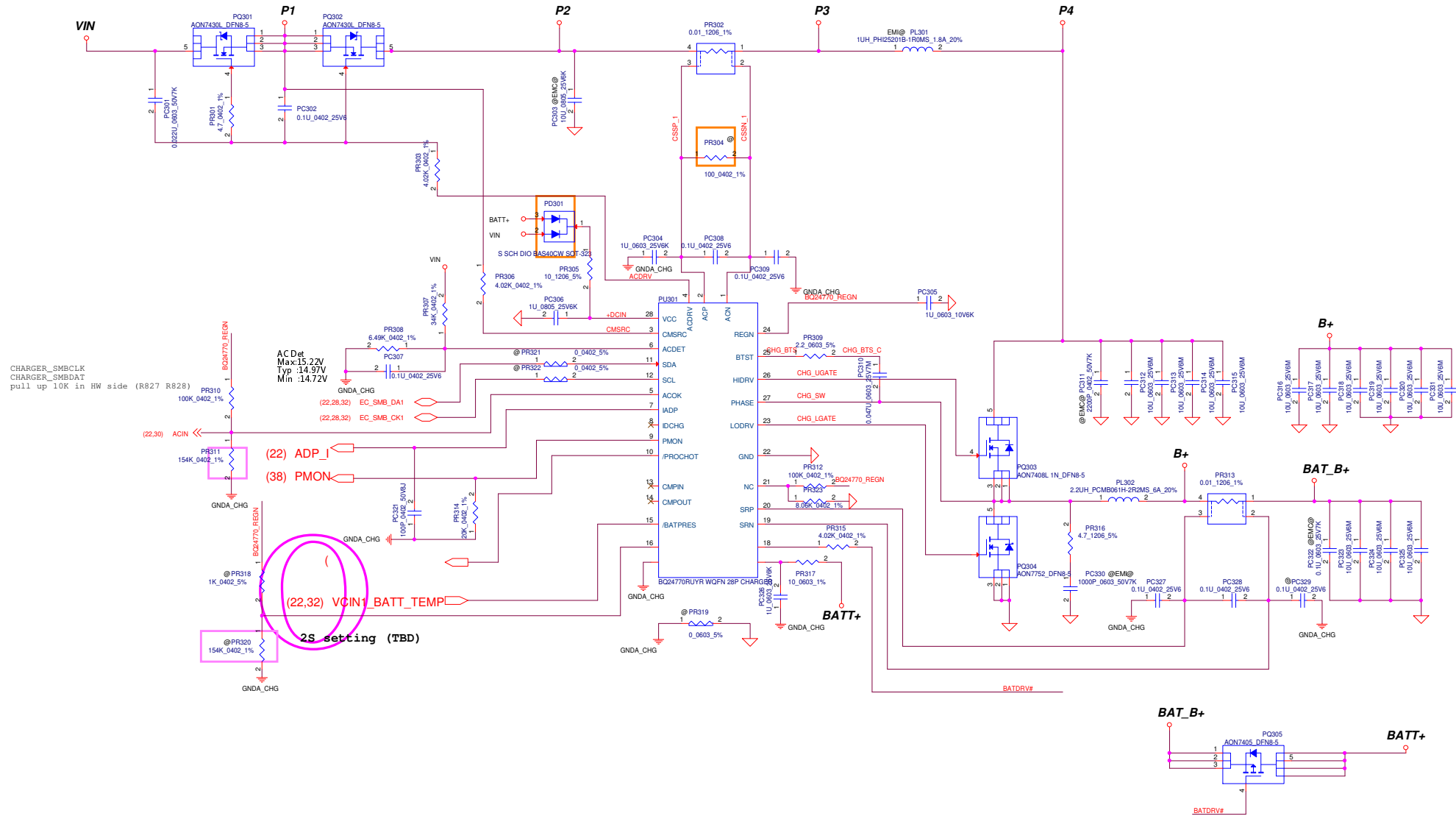
**65W(UMA): 85W active W recovery**

20120314  
 Change to +EC\_VCCA from +3VLP




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DELL CONFIDENTIAL/PROPRIETARY

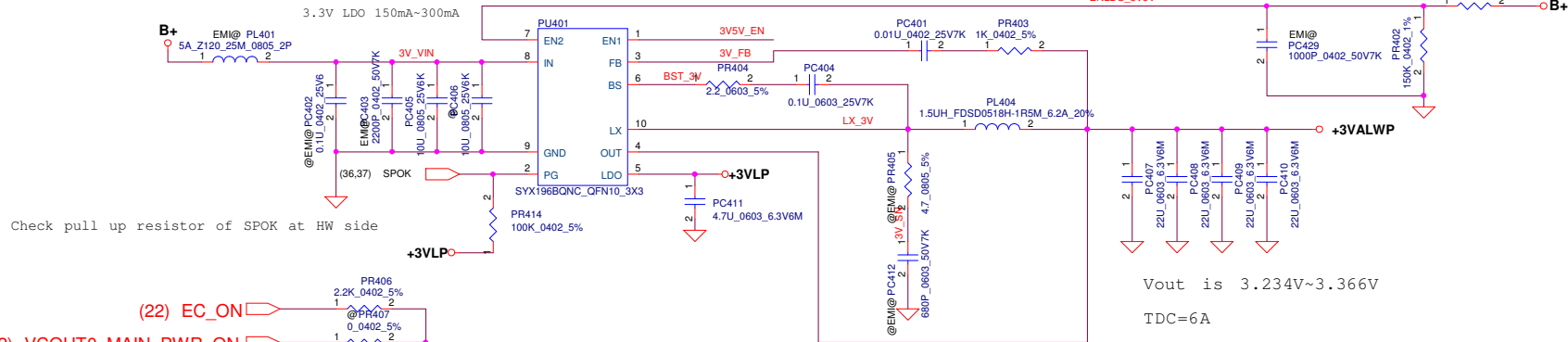
		Compal Electronics, Inc.	
		Charger	
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# Module model information

SYX196B\_V4.mdd

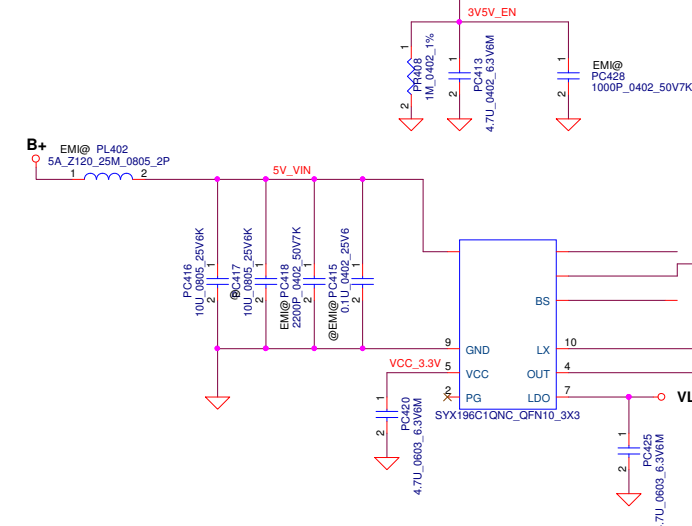
EN1 and EN2 don't floating



Check pull up resistor of SPOK at HW side

(22) EC\_ON

(22) VCOUT0\_MAIN\_PWR\_ON



# Module model information

SYX196C\_V4.mdd

5V LDO 150mA~300mA

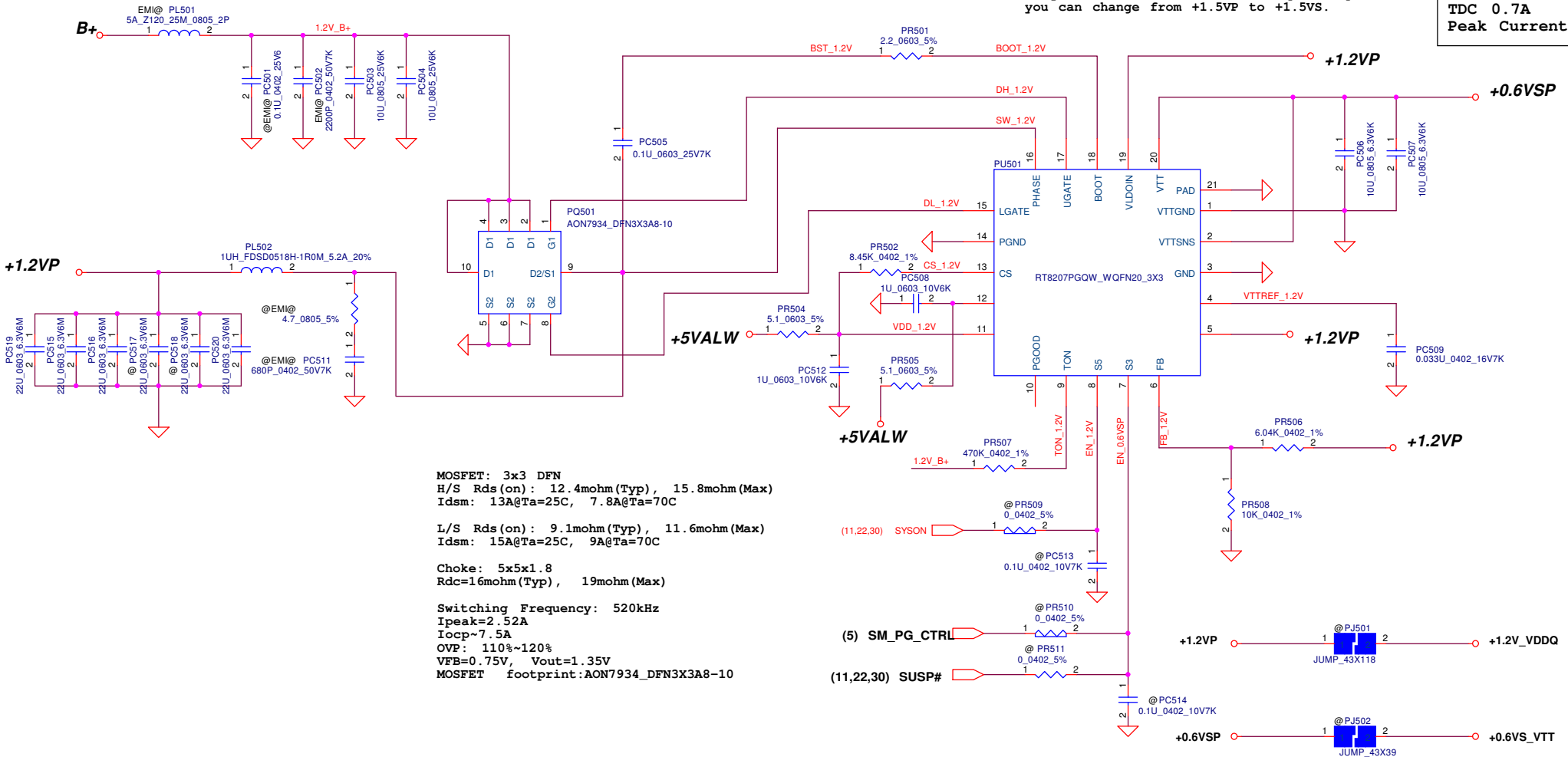
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/10	Deciphered Date	2017/04/10	Title	PWR-3VALW/5VALW
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# Module model information

RT8207M\_V1.mdd For Single layer  
RT8207M\_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.  
If you have +1.5V and +0.75V sequence question,  
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%  
TDC 0.7A  
Peak Current 1A

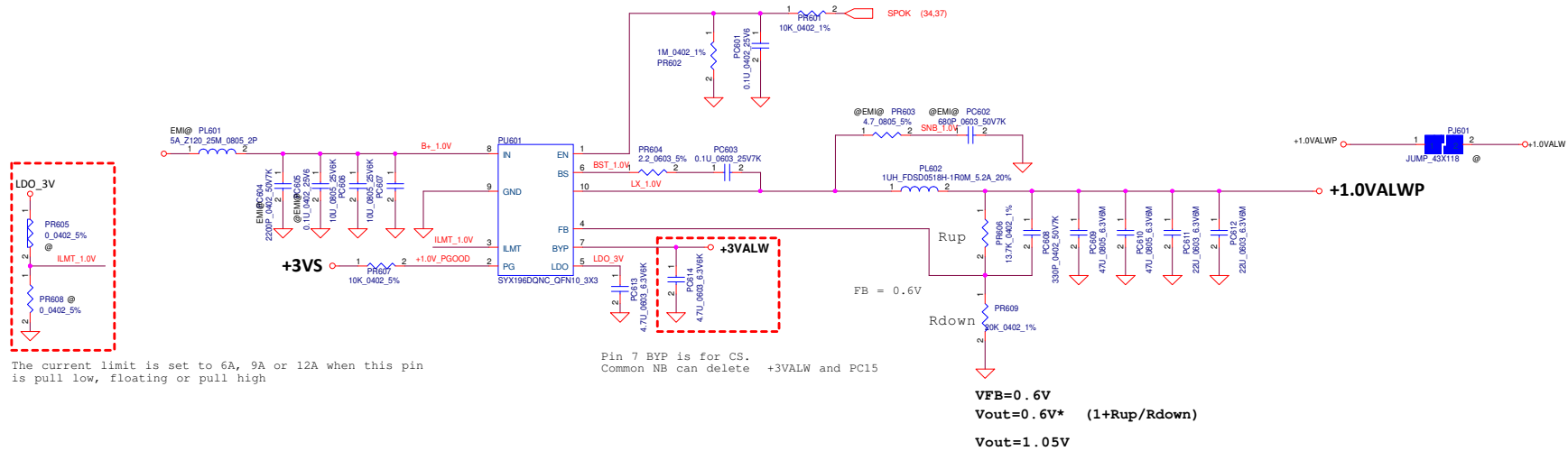


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Size		Document Number		YOGA Paganini	
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Module model information

SYX196D\_V3.mdd

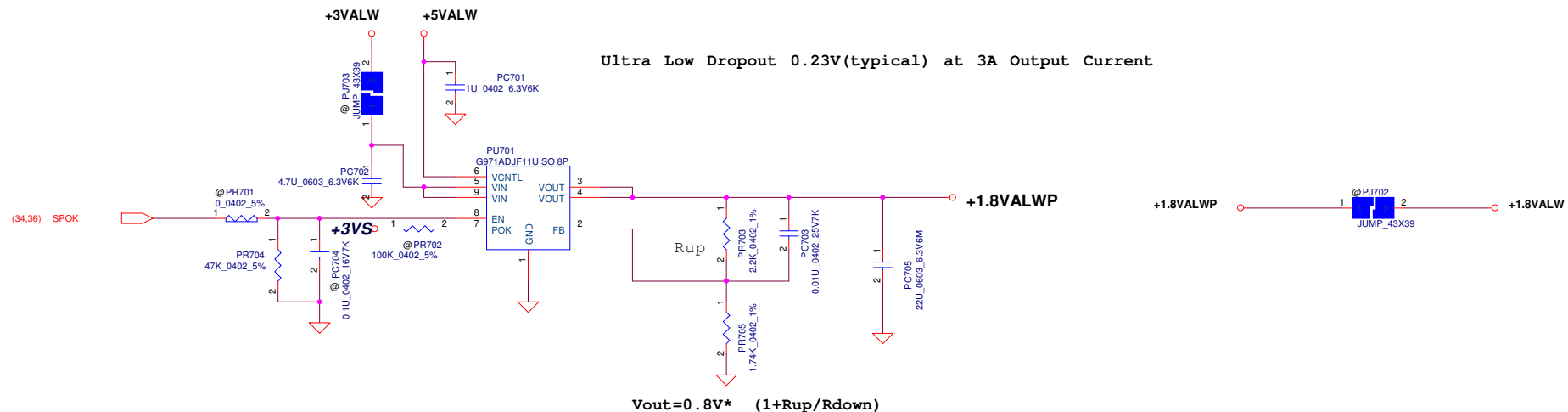
EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



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# Module model information

APL5930\_V2.mdd



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## CPU CORE

Module model information

NCP81208_U22_V1A.mdd	for	IC	portion
NCP81208_U22_V1B.mdd	for	SW	portion

```
IccMAX@SA= 5A
RiccMAX@SA= 15.8K --->PRI65

RiccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=31.6K --->PRI14

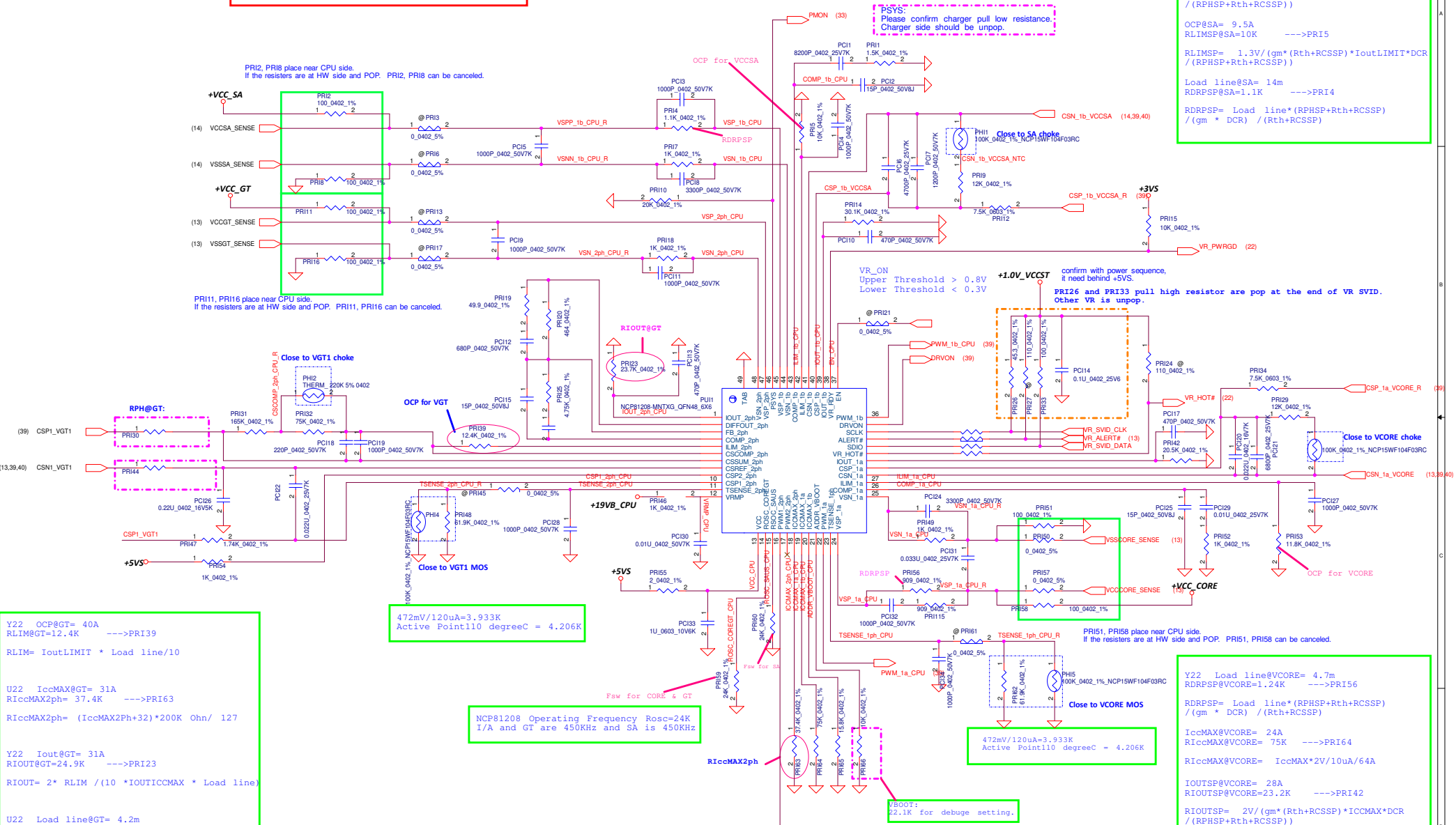
RIOUTSP= 2V/(gm*(Rth+RCSSP))*IccMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@SA= 9.5A
RLIMSP@SA=10K --->PRI5

RLIMSP= 1.3V/(gm*(Rth+RCSSP))*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Load line@SA= 14m
RDRPSP@SA=1.1K --->PRI4

RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)
```



```

Y22  OCP@GT= 40A
RLIM@GT=12.4K  ---->PRI39

RLIM= IoutLIMIT * Load line/10

U22  IccMAX@GT= 31A
RiccMAX2ph= 37.4K  ---->PRI63

RiccMAX2ph= (IccMAX2Ph+32)*200K Ohm/ 127

Y22  Iout@GT= 31A
RIOUT@GT=24.9K  ---->PRI23

RIOUT= 2* RLIM / (10 * IOUTICCMAX * Load line)

U22  Load line@GT= 4.2m
RPH@GT=210K  ---->PRI30

Load line= (RC52+(RC51*Rth/(RC51+Rth)))
*IOUTTOTAL * DCR/RPH

```

472mV/120uA=3.933K  
Active Point110 degreeC = 4.206K

NCP81208 Operating Frequency Rosc=24K  
I/A and GT are 450KHz and SA is 450KHz

472mV/120uA=3.933K  
Active Point110 degreeC = 4.206K

```

Y22 Load line@VCORE= 4.7m
RDRPSP@VCORE=1.24K ---->PRI56

RDRPSP= Load line* (RHPSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

IccMAX@VCORE= 24A
RiccMAX@VCORE= 75K ---->PRI64

RiccMAX@VCORE= IccMAX*2V/10uA/64A

IOUTSP@VCORE= 28A
RIOUTSP@VCORE=23.2K ---->PRI42

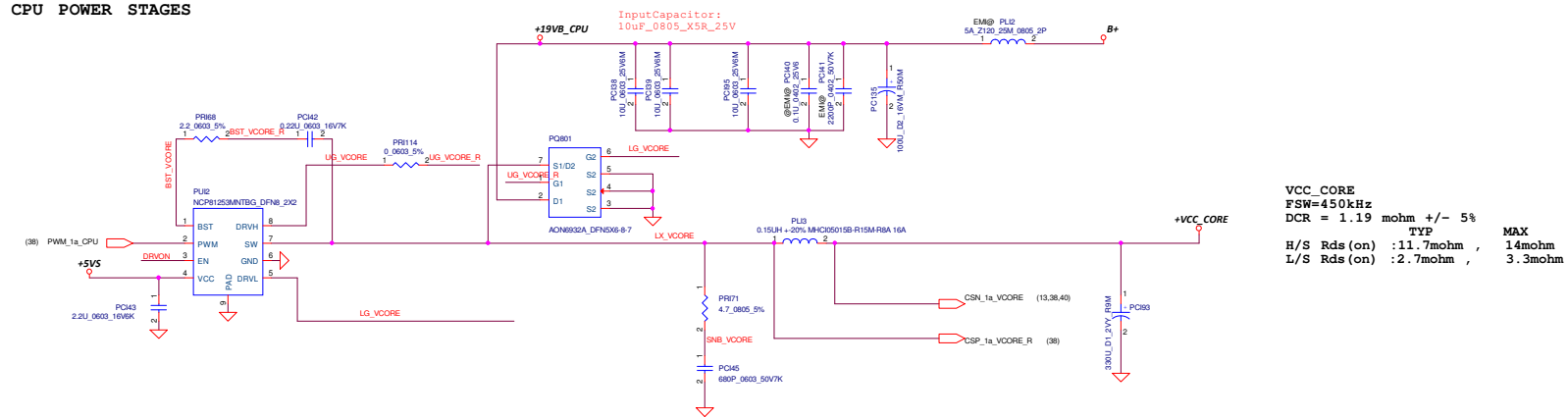
RIOUTSP= 2V/(gm*(Rth+RCSSP) *ICCMAX*DCR
/(RHPSP+Rth+RCSSP))

OCPE@VCORE= 35A
RLIMSP@VCORE=11.8K ---->PRI53

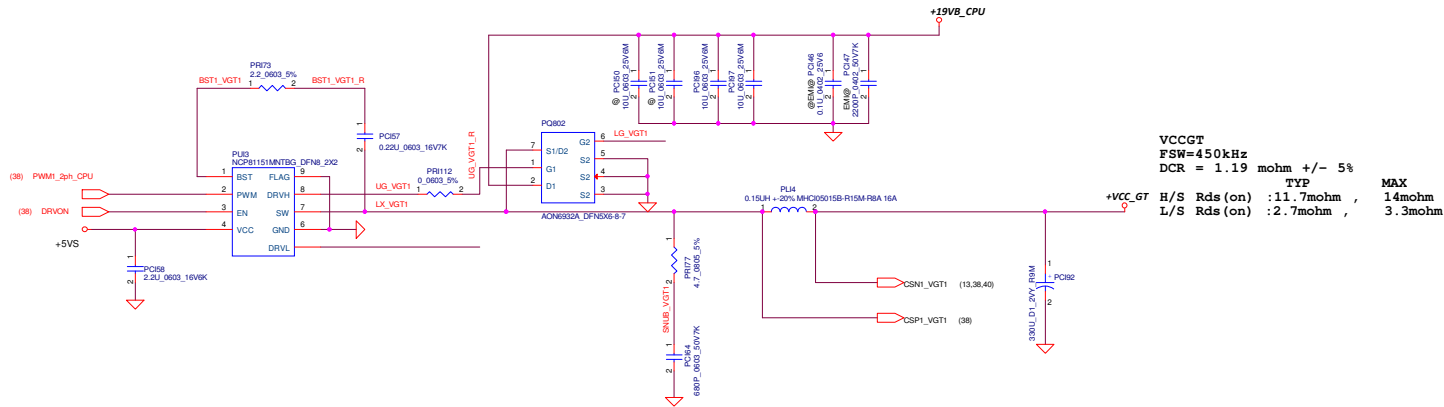
RLIMSP= 1.3V/(gm*(Rth+RCSSP) *IoutLIMIT*DCR
/(RHPSP+Rth+RCSSP))

```

## CPU POWER STAGES

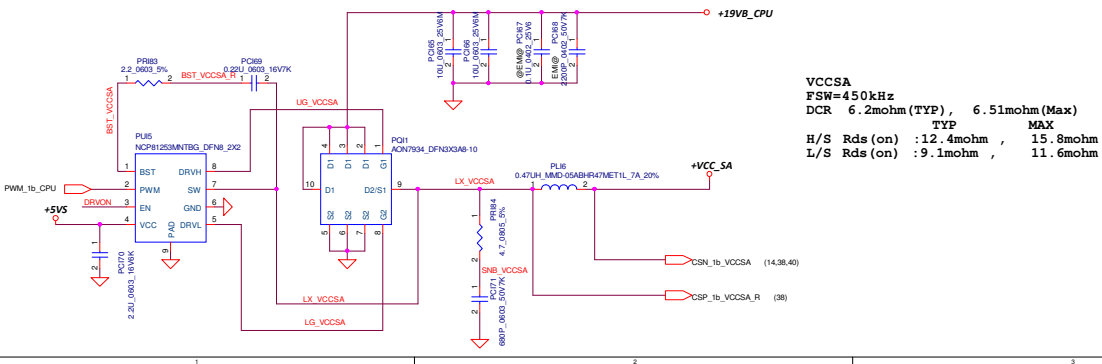


VCC_CORE		
FSW=450kHz		
DCR = 1.19 mohm +/- 5%		
	TYP	MAX
H/S Rds(on)	:11.7mohm ,	14mohm
L/S Rds(on)	:2.7mohm ,	3.3mohm



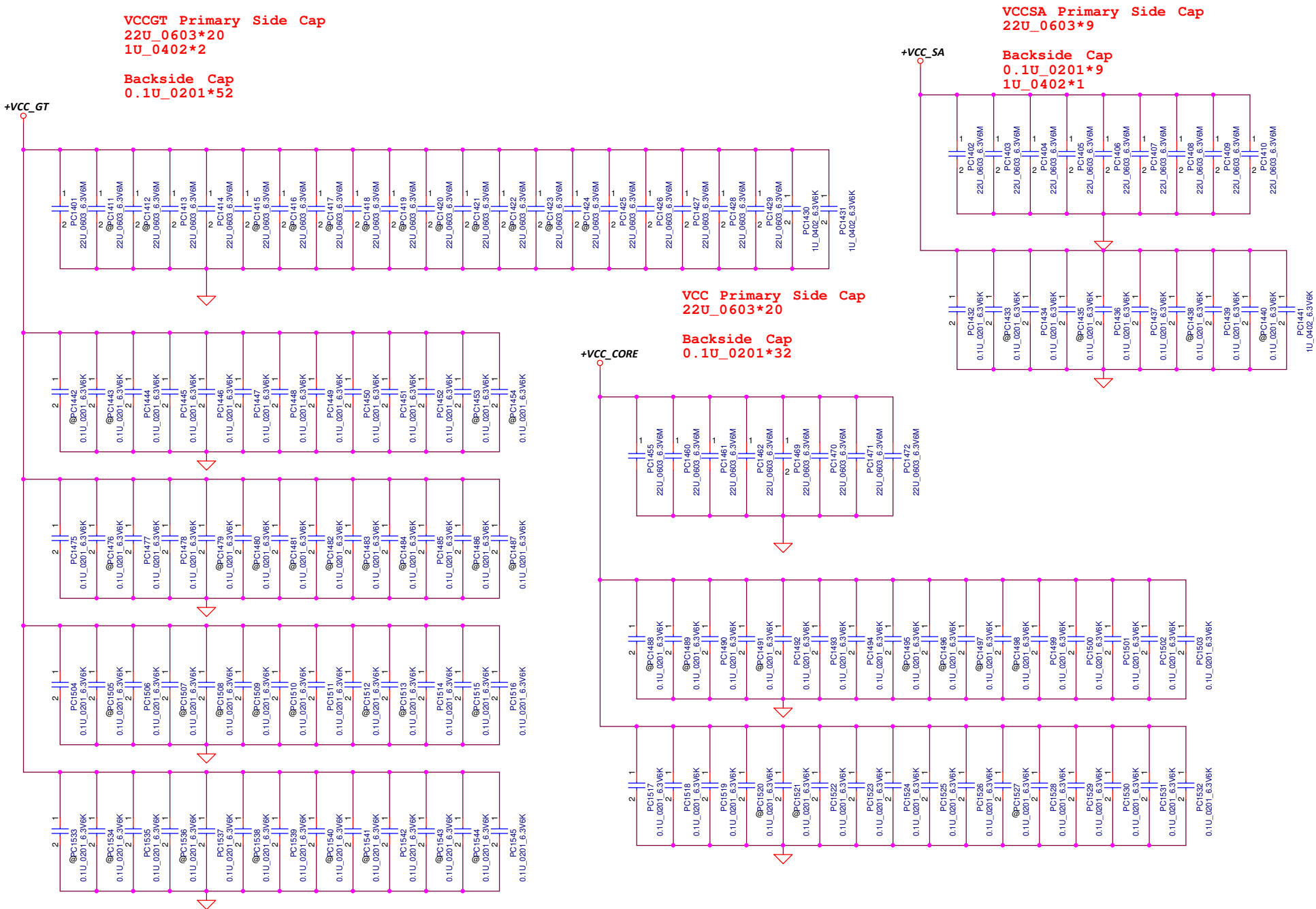
VCCGT  
FSW=450kHz  
DCR = 1.19 mohm +/- 5%

	TYP	MAX
H/S Rds (on)	:11.7mohm ,	14mohm
L/S Rds (on)	:2.7mohm ,	3.3mohm



VCCSA  
FSW=450kHz  
DCR 6.2mohm (TYP), 6.51mohm (Max)  
TYP MAX  
H/S Rds (on) :12.4mohm , 15.8mohm  
L/S Rds (on) :9.1mohm , 11.6mohm

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Item	Reason for change	PAGE	Modify List	Date	Phase
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## Version change list (P.I.R. List)

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for HW

Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	Reducce In-rush current	P.30	change UC8 load switch	2015-04-30	EVT-DVT	verify OK
2	EC request	P.33	modify pass through mode net name at power side(ACIN)	2015-04-30	EVT-DVT	verify OK
3	EMI request	P.26	change LA5,LA6,LA7,LA8 from 0 ohm to 120 ohm bead	2015-04-30	EVT-DVT	EA pass
4	SW request	P.10	swap USB 2.0 sub and touch panel USB 2.0 signals	2015-04-30	EVT-DVT	verify OK
5	ESD request		mount C188,C194,C195,C198,C199,C200,C5274	2015-04-30	EVT-DVT	EA pass
6	Vendor request	P.22	add R207 on ME_EN	2015-04-30	EVT-DVT	verify OK
7	Reserved Thermal solution	P.18	add DDR_TEMP net and add RD79, RHD1	2015-04-30	EVT-DVT	verify OK
8	Intel review feedback	P.17	add DDR_A_CKE2, DDR_A_CKE3 nets and add RD80, RD81	2015-04-30	EVT-DVT	verify on DVT
9	Intel review feedback	P.18	add DDR_B_CKE2, DDR_B_CKE3 nets and add RD82, RD83	2015-04-30	EVT-DVT	verify on DVT
10	EC request	P.22	swap DDR_TEMP/ TAB_SW# to EC pin 73 and pin 89, respectively	2015-05-05	EVT-DVT	verify OK
11					EVT-DVT	
12					EVT-DVT	
Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	Intel PDG update	P.12	add CC76 on +1.0V_CLK5_F24NS	2015-06-29	DVT-PVT	verify on PVT
2	0 ohm part count reduce		R187,R195,R323,R324,R11,RS16,RS17,RC90,R2107, R2108,RS18,R5216, R1460, R17, R132, R1518	2015-06-29	DVT-PVT	verify OK
3	Unify battery internal resistor		RC39 change from 806 ohm to 0 ohm			
4	Intel PDG update	P.05	tie DDR0_ALERT#/ DDR1_ALERT# to GND	2015-06-29	DVT-PVT	verify on PVT
5	ESD request	P.28	reserved D106 on USB20_P5/ USB20_N5	2015-06-29	DVT-PVT	verify on PVT
6					DVT-PVT	
7					DVT-PVT	
8					DVT-PVT	
9					DVT-PVT	
10					DVT-PVT	
11					DVT-PVT	
12					DVT-PVT	
Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	WLAN (WiFi) Radio Interference at 5.76GHz	P.12	change RC159 from R-short to 0402 bead	2015-08-03	PVT-SOVP	verify OK
2	modify co-lay design for DFX/MFG resuest		cancel L30,L31,L32,L33,L44,L45,L55,R173,R174, R175,R176,R177,R178,R5223 and R5224	2015-08-03	PVT-SOVP	verify OK
3					PVT-SOVP	
4					PVT-SOVP	

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[Power ON Sequence] (TBC)

